Government Polytechnic Vaishali, Bihar

Under Department of Science, Technology and Technical Education, Bihar
Affiliated By State Board of Technical Education

LAB MANUAL

FUNDAMENTALS OF ELECTRONICS ENGINEERING

SUBJECT CODE – P2421102

Government Polytechnic Vaishali

Department of Electrical Engineering

Vision

To nurture industry-ready and ethically responsible diploma engineers in Electrical Engineering, equipped with modern technical skills, digital competence, and adaptability to support evolving industrial, infrastructural, and societal needs.

Mission

M1: To provide a student-centric and outcome-based learning ecosystem that integrates classroom instruction with modern laboratories, simulation software, digital learning platforms, and hands-on practices for effective knowledge acquisition.

M2: To impart application-oriented technical skills in electrical machines, power distribution systems, industrial wiring, control circuits, basic automation, and testing instruments, emphasizing safety standards, quality practices, and the use of contemporary tools and technologies.

M3: To strengthen industry readiness, employability, entrepreneurship, and preparedness for higher education through industry–institute interaction, internships, field exposure, expert lectures, skill development programs, guidance, innovation support, and awareness of emerging trends such as energy efficiency, renewable integration, and smart electrical systems.

M4: To foster professional ethics, teamwork, communication skills, problem-solving ability, environmental consciousness, and lifelong learning attitude, enabling diploma holders to contribute responsibly to industry, society, and national development.

Practical/Lab Session Outcomes (LSOs)

S.NO	Laboratory Experiment	Lab Session Outcomes
1	Test the performance of Zener Diode.	Identify the IC number of Zener diode. Build the circuit using Zener diode. Plot the V-I characteristic of Zener diode.
2	Test the functionality of Half wave rectifier.	Build the circuit of Half wave rectifier using diode on breadboard/ trainer kit. Verify the output waveform of Half wave rectifier.
3	Test the functionality of Full wave rectifier.	Build the circuit of Full wave rectifier using diode on breadboard/ trainer kit. Verify the output waveform of Full wave rectifier.
4	Construct the power supply of +5V.	Build the circuit of power supply using IC 7805. Verify the output of power supply.
5	Construct the power supply of -5V.	Build the circuit of power supply using IC 7905. Verify the output of power supply.
6	Identify the given transistor.	List the IC number of BJTs provided. Identify the terminal of BJT using multimeter. Verify the terminal of BJT with data sheet.
7	Test the input and output characteristics of the CE amplifier.	Build the CE configuration circuit Verify the input and output characteristics.
8	Test the input and output characteristics of the CC amplifier.	Build the CC configuration circuit. Verify the input and output characteristics.

9	Test the input and output characteristics of the CB amplifier.	Build the CB configuration circuit. Verify the input and output characteristics.
10	Measure the voltage gain and current gain of CE configuration.	Build the CE configuration circuit. Measure the voltage gain & current gain of the CE configuration.
11	Measure the voltage gain and current gain of CC configuration.	Construct the CC configuration circuit. Measure the voltage & current gain of the CC configuration.
12	Measure the voltage gain and current gain of CB configuration.	Construct the CB configuration circuit. Measure the voltage & current gain of the CB configuration.
13	Test the functionality of given logic gates using ICs.	List the IC number of different types of logic gates. Verify the truth table of identified logic gate.
14	Implement logic gates using universal NAND gate IC.	Build the circuit on breadboard for making AND gate using NOR gate. Verify the truth table of the developed AND gate. Build the circuit on breadboard similarly for other gates using NOR gate. Verify the truth table of the developed gate.
15	Implement logic gates using universal NOR gate IC.	Build the circuit on breadboard for making AND gate using NOR gate. Verify the truth table of the developed AND gate. Build the circuit on breadboard similarly for other gates using NOR gate. Verify the truth table of the developed gate.

16	Implement Half adder and Half subtractor using basic gates.	Build the circuit of Half adder using basic gates on breadboard. Test the functionality of Half Adder. Build the circuit of Half Subtractor on breadboard. Test the functionality of Half Subtractor.
17	Implement Full Adder using basic gates.	Build the circuit of Full Adder using basic gates on breadboard. Check the result of binary addition on the developed circuit.
18	Implement Full Subtractor using basic gates.	Build the circuit of full subtractor using NOR gate on breadboard. Check the result of binary subtraction on the developed circuit.
19	Test the functionality of multiplexer on trainer kit.	Build the circuit connection of multiplexer on trainer kit. Test whether the particular input line is available at output for given data select line.
20	Build and test the functionality of de multiplexer on trainer kit.	Build the circuit connection of De-multiplexer. Test whether the given data available at input is distributed correctly to output for given data select line.
21	Verify the function of SR flip-flop using NAND/NOR gate.	Build the circuit of SR flip-flop on breadboard. Verify the characteristic table of SR flip-flop.
22	Test the functionality of D and T flip-flop using IC 7476.	Construct the circuit diagram of D and T flip flop on breadboard. Test the functionality of D and T flip-flop.
23	Test the functionality of DAC and ADC using IC.	List the IC number of DAC and ADC. Test its functionality.

LIST OF EXPERIMENTS

1	Test the performance of Zener Diode.
2	Test the functionality of Half wave rectifier.
3	Test the functionality of Full wave rectifier.
4	Construct the power supply of +5V.
5	Construct the power supply of -5V.
6	Identify the given transistor.
7	Test the input and output characteristics of the CE amplifier.
8	Test the input and output characteristics of the CC amplifier.
9	Test the input and output characteristics of the CB amplifier.
10	Measure the voltage gain and current gain of CE configuration.
11	Measure the voltage gain and current gain of CC configuration.
12	Measure the voltage gain and current gain of CB configuration.
13	Test the functionality of given logic gates using ICs.
14	Implement logic gates using universal NAND gate IC.

15	Implement logic gates using universal NOR gate IC.
16	Implement Half adder and Half subtractor using basic gates.
17	Implement Full Adder using basic gates.
18	Implement Full Subtractor using basic gates.
19	Test the functionality of multiplexer on trainer kit.
20	Build and test the functionality of de multiplexer on trainer kit.
21	Verify the function of SR flip-flop using NAND/NOR gate.
22	Test the functionality of D and T flip-flop using IC 7476.
23	Test the functionality of DAC and ADC using IC.

PRACTICAL OUTCOMES

CO	Statement
1	Use diode for rectification and voltage regulation.
2	Test the functionality of electronic circuit having transistor as a component.
3	Minimize the Boolean expressions and implement it using logic gates.
4	Test simple combinational and sequential circuits.
5	Use data converters and memory in digital electronic systems.

PROGRAM EDUCATIONAL OBJECTIVES (PEO)

PEO No.	Program Educational Objectives Statements
PEO1	To prepare diploma holders with a strong foundation in electrical engineering fundamentals and state-of-the-art technologies, enabling continuous learning, skill upgradation, and adaptability to emerging industrial and technological trends.
PEO2	To develop professionally responsible diploma holders with effective communication skills, leadership qualities, ethical values, and the ability to work efficiently as individuals and as members of multidisciplinary teams.
PEO3	To enhance employability by providing industry-oriented training, hands-on experience, and exposure through industrial visits, internships, seminars, workshops, and interaction with industry professionals and academicians.
PEO4	To enable diploma holders to apply project-based learning, modern tools, and innovative approaches to develop solutions addressing technical, socio-economic, and environmental challenges in a sustainable and socially responsible manner.

PROGRAM SPECIFIC OUTCOMES

PSO1: Design, Install, operate, and troubleshoot electrical systems, machines and power circuits using modern tools while adhering to safety standards and environmental consideration.

PSO2: Work effectively in multidisciplinary teams to solve real-time electrical engineering problems and communicate technical information clearly and professionally.

PROGRAM OUTCOMES (POS)

P01: Basic and Discipline specific knowledge: Apply knowledge of basic mathematics, science and engineering fundamentals and engineering specialization to solve the engineering problems.

PO2: Problem analysis: Identify and analyse well-defined engineering problems using codified standard methods.

PO3: Design/ development of solutions: Design solutions for well-defined technical problems and assist with the design of systems components or processes to meet specified needs.

P04: Engineering Tools, Experimentation and Testing: Apply modern engineering tools and appropriate technique to conduct standard tests and measurements.

PO5: Engineering practices for society, sustainability and environment: Apply appropriate technology in context of society, sustainability, environment and ethical practices.

PO6: Project Management: Use engineering management principles individually, as a team member or a leader to manage projects and effectively communicate about well-defined engineering activities.

PO7: Life-long learning: Ability to analyze individual needs and engage in updating in the context of technological changes.

EXPERIMENT NO: 01

Test the performance of Zener Diode.

1. Aim

To study the reverse-bias V-I characteristics of a Zener diode and to verify its voltage regulation (constant voltage) property.

2. Theory

A Zener diode is a heavily doped p-n junction diode designed to operate safely in the reverse breakdown region. Under forward bias it behaves like an ordinary silicon diode, conducting after about 0.7V. Under reverse bias, as the applied voltage is increased, the diode current remains extremely small (leakage current) until a specific voltage called the Zener breakdown voltage (Vz) is reached. Beyond this point, the current increases sharply for a very small increase in voltage, and the diode maintains an almost constant voltage across its terminals over a wide current range.

Breakdown in a Zener diode occurs by two mechanisms. For diodes with Vz below about 5V, breakdown occurs due to the Zener effect, where a very strong electric field across the narrow depletion region directly pulls valence electrons out of their covalent bonds. For diodes with Vz above about 5V, breakdown occurs due to the Avalanche effect, in which minority carriers accelerated by the electric field collide with lattice atoms and generate additional electron-hole pairs through impact ionisation.

Key parameters: Zener breakdown voltage (Vz), knee current (Izk) — the minimum current required to sustain regulation, maximum current (Izmax), and dynamic (Zener) resistance Rz = ΔVz/ΔIz, which is ideally very small. Because Vz stays nearly constant despite large changes in Iz, the Zener diode is widely used as a voltage reference and simple shunt voltage regulator, provided a series resistor is used to limit current.

3. Practical Set-up / Circuit Diagram

Fig 1: Circuit Diagram - Zener Diode V-I Characteristics

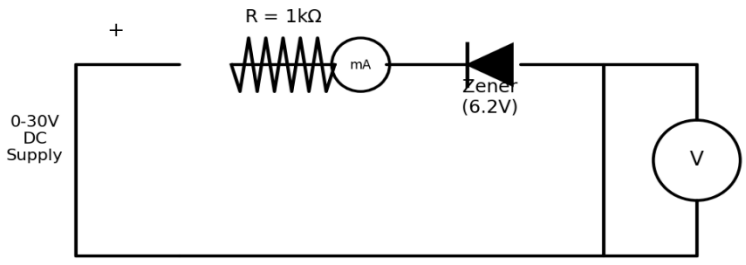

Fig. 1.1: Test circuit for Zener diode reverse-bias V-I characteristics

The Zener diode is connected in reverse bias in series with a current-limiting resistor R across a variable DC supply. A milliammeter (mA) is connected in series to measure Iz and a voltmeter (V) is connected across the Zener diode to measure Vz.

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	Zener Diode	6.2V, 500mW	1
2	Resistor	1kΩ, 1/2W	1
3	Regulated DC Power Supply (RPS)	0-30V	1
4	Digital Multimeter / Voltmeter	0-20V DC	1
5	Milliammeter	0-50mA DC	1
6	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Connect the Zener diode strictly in reverse bias as per the circuit diagram; check cathode/anode markings before connecting.
- Do not exceed the maximum permissible reverse current (Izmax) of the diode.
- Increase the supply voltage gradually in small steps; do not apply sudden high voltage.
- Ensure meter ranges are selected correctly before switching on the supply.
- Avoid loose connections on the breadboard.
- Switch off the supply immediately if the diode becomes unusually hot.

6. Procedure

1. Connect the circuit as shown in Fig. 1.1 with the Zener diode in reverse bias through the series resistor R.
2. Keep the DC supply voltage at 0V initially and switch on the circuit.
3. Increase the input voltage gradually in small steps (e.g., 0.5V or 1V steps).
4. At each step, note down the voltmeter reading (Vz) across the Zener diode and the milliammeter reading (Iz).
5. Continue till the breakdown (knee) region is crossed and note additional readings after breakdown, where Vz remains nearly constant while Iz increases rapidly.
6. Tabulate all readings and plot a graph of Vz (X-axis) versus Iz (Y-axis).
7. Identify the knee point and the Zener breakdown voltage from the graph.

7. Observations and Calculations (Observations Table)

S.No.	Supply Voltage (V)	Zener Voltage Vz (V)	Zener Current Iz (mA)	Remarks
1				
2				
3				
4				
5				
6				

Calculations: Dynamic resistance in breakdown region, Rz = ΔVz / ΔIz (calculated between two points in the breakdown region)

8. Results

The reverse-bias V-I characteristics of the given Zener diode were plotted. The Zener breakdown voltage was found to be approximately Vz = ____ V, and the diode was observed to maintain this voltage nearly constant over the tested range of reverse current, confirming its voltage regulation property.

9. Viva Book

1. What is a Zener diode and how does it differ from an ordinary diode?
2. Explain the Zener effect and the Avalanche effect of breakdown.
3. Why must a series resistor always be used with a Zener diode?
4. Define knee current and dynamic resistance of a Zener diode.
5. What are the practical applications of a Zener diode?
6. What happens if the reverse current exceeds Izmax?

EXPERIMENT NO: 02

To Test the Functionality of a Half Wave Rectifier

1. Aim

To study and test the functionality of a half wave rectifier circuit and to observe its input-output waveforms, DC output voltage, and ripple factor, with and without a filter capacitor.

2. Theory

A half wave rectifier is the simplest type of rectifier circuit that converts an alternating current (AC) input into a pulsating unidirectional (DC) output using a single p-n junction diode. During the positive half cycle of the AC input, the diode is forward biased and conducts, allowing current to flow through the load resistor RL, and the output follows the input waveform. During the negative half cycle, the diode becomes reverse biased and does not conduct, so no current flows through the load and the output voltage is zero.

As a result, the output waveform consists of only the positive half cycles of the input, repeating once every input cycle. This makes the half wave rectifier inefficient, with a theoretical maximum efficiency of about 40.6% and a high ripple factor of about 1.21, meaning the DC output still contains a large AC component.

A filter capacitor connected across the load charges to nearly the peak voltage during conduction and discharges slowly through RL during the non-conducting interval, which reduces the ripple and raises the average DC output voltage, giving a smoother, more usable DC output.

3. Practical Set-up / Circuit Diagram

Fig 2: Circuit Diagram - Half Wave Rectifier

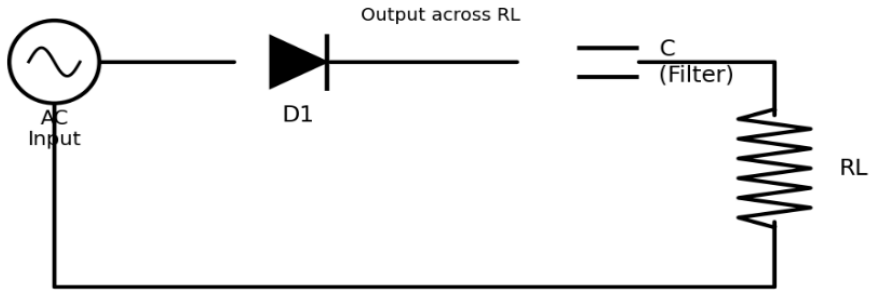

Fig. 2.1: Half wave rectifier circuit with capacitor filter

A step-down transformer provides low-voltage AC to the diode D1, which is connected in series with the load RL. The filter capacitor C is connected in parallel with RL, and the output is taken across RL.

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	Step-down Transformer	230V/6-0-6V or 12V, 1A	1
2	Rectifier Diode	IN4007	1
3	Load Resistor RL	1kΩ, 1/2W	1
4	Filter Capacitor	100µF/470µF, 25V	1
5	Cathode Ray Oscilloscope (CRO)	20-30 MHz	1
6	Digital Multimeter	0-750V AC/DC	1
7	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Check the polarity of the diode and the electrolytic filter capacitor before connecting.
- Ensure the transformer secondary voltage is within the safe input rating of the diode.
- Do not touch the primary (mains) side terminals of the transformer.
- Set the CRO to the correct volts/division and time/division before taking readings.
- Ensure common ground reference between the CRO probe and the circuit.
- Switch off supply before changing any circuit connection.

6. Procedure

- Connect the circuit as shown in Fig. 2.1 without the filter capacitor initially.
- Switch on the AC mains supply to the transformer primary.
- Observe the input AC waveform on channel 1 of the CRO and the output waveform across RL on channel 2.
- Note the peak input voltage (Vm) and observe that the output appears only during the positive half cycle.
- Measure the DC output voltage (Vdc) and the rms value using a multimeter.
- Now connect the filter capacitor C across RL and again observe the output waveform on the CRO.
- Note the reduction in ripple and the increase in average DC output voltage.
- Calculate the ripple factor from the observed rms and DC values.

7. Observations and Calculations (Observations Table)

S.No.	Condition	Vrms input (V)	Vm peak (V)	Vdc output (V)	Ripple Factor
1	Without Filter				
2	With Filter				

Calculations: Without filter, $V_{dc} = V_m/\pi$; Ripple Factor $\gamma = \sqrt{[(V_{rms}/V_{dc})^2 - 1]}$; Theoretical $\gamma \approx 1.21$. With filter, $V_{dc} \approx V_m - (I_{dc} / (2 \cdot f \cdot C))$.

8. Results

The half wave rectifier circuit was constructed and tested successfully. The output waveform was observed to contain only the positive half cycles of the input. Without the filter capacitor, the measured ripple factor was found close to the theoretical value of 1.21. With the filter capacitor connected, the ripple was significantly reduced and the DC output voltage increased, confirming the smoothing action of the filter.

9. Viva Book

1. What is rectification and why is it needed?
2. Derive the expression for Vdc of a half wave rectifier.
3. What is the Peak Inverse Voltage (PIV) for a half wave rectifier?
4. Define ripple factor and state its theoretical value for a half wave rectifier.
5. What is the maximum theoretical efficiency of a half wave rectifier?
6. How does a filter capacitor improve the output of a rectifier?

EXPERIMENT NO: 03

To Test the Functionality of a Full Wave (Bridge) Rectifier

1. Aim

To study and test the functionality of a full wave bridge rectifier circuit and to observe its input-output waveforms, DC output voltage, ripple factor, and efficiency, with and without a filter capacitor.

2. Theory

A full wave bridge rectifier uses four diodes connected in a bridge (diamond) configuration to convert both half cycles of an AC input into a unidirectional pulsating DC output, without requiring a centre-tapped transformer. During the positive half cycle of the AC input, diodes D1 and D3 become forward biased and conduct, while D2 and D4 remain reverse biased. During the negative half cycle, the polarity reverses, so D2 and D4 conduct while D1 and D3 remain reverse biased. In both cases, current is directed through the load RL in the same direction, so the output consists of a series of positive half-cycle pulses occurring at twice the input frequency.

Because both half cycles of the input contribute to the output, the full wave bridge rectifier has a much higher theoretical efficiency (~81.2%) and a lower ripple factor (~0.48) compared to the half wave rectifier. Connecting a filter capacitor across the load further smooths the output by charging near the peak voltage and discharging slowly between successive pulses, which are now more closely spaced than in a half wave rectifier, giving a much lower ripple.

3. Practical Set-up / Circuit Diagram

Fig 3: Circuit Diagram - Full Wave Bridge Rectifier

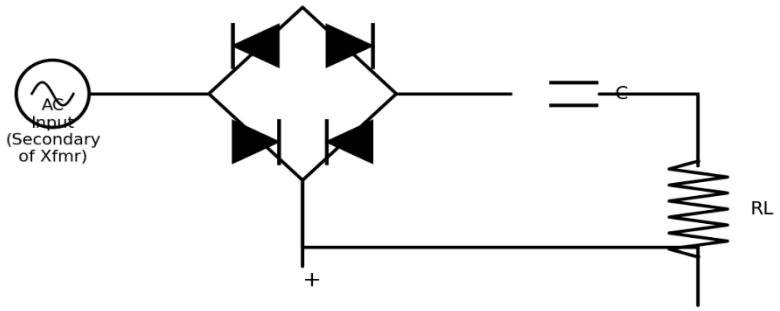

Fig. 3.1: Full wave bridge rectifier circuit with capacitor filter

The secondary of the step-down transformer is connected to two opposite corners of the diode bridge (D1-D4). The load RL and filter capacitor C are connected across the remaining two corners, which form the DC output terminals.

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	Step-down Transformer	230V/12V, 1A	1
2	Rectifier Diodes	IN4007	4
3	Load Resistor RL	1kΩ, 1/2W	1
4	Filter Capacitor	470µF/1000µF, 25V	1
5	Cathode Ray Oscilloscope (CRO)	20-30 MHz	1
6	Digital Multimeter	0-750V AC/DC	1
7	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Connect all four diodes in the bridge with correct polarity as per the circuit diagram.
- Ensure the transformer secondary voltage rating matches the diode and capacitor voltage ratings.
- Do not touch mains-side terminals of the transformer while the supply is switched on.
- Check the polarity of the electrolytic filter capacitor before connecting.
- Verify CRO ground connection is common with the circuit ground.
- Switch off the supply before altering any connections.

6. Procedure

- Connect the four diodes in bridge configuration and complete the circuit as shown in Fig. 3.1, without the filter capacitor initially.
- Switch on the AC supply and observe the input waveform and the rectified output waveform across RL on the CRO.
- Verify that the output waveform contains pulses corresponding to both half cycles of the input, at twice the input frequency.
- Measure the peak output voltage (Vm), DC output voltage (Vdc) and rms voltage using the multimeter.
- Now connect the filter capacitor C across RL and again observe the output waveform.
- Note the significant reduction in ripple and the increase in average DC output voltage.
- Calculate the ripple factor and rectifier efficiency from the observed values.

7. Observations and Calculations (Observations Table)

S.No.	Condition	Vrms input (V)	Vm peak (V)	Vdc output (V)	Ripple Factor
1	Without Filter				
2	With Filter				

Calculations: Without filter, $V_{dc} = 2V_m/\pi$; Ripple Factor $\gamma = \sqrt{[(V_{rms}/V_{dc})^2 - 1]}$; Theoretical $\gamma \approx 0.48$; Theoretical efficiency ≈ 81.2%.

8. Results

The full wave bridge rectifier circuit was constructed and tested successfully. The output waveform was observed to contain pulses from both half cycles of the input at twice the input frequency. The measured ripple factor without filter was found close to the theoretical value of 0.48, which reduced further after connecting the filter capacitor, confirming higher efficiency and lower ripple compared to the half wave rectifier.

9. Viva Book

1. Why is a bridge rectifier preferred over a centre-tapped full wave rectifier?
2. Explain the conduction of diodes during positive and negative half cycles in a bridge rectifier.
3. Derive the expression for Vdc of a full wave rectifier.
4. What is the PIV rating required for diodes in a bridge rectifier?
5. Compare the ripple factor and efficiency of half wave and full wave rectifiers.
6. What is the output ripple frequency of a full wave rectifier for a 50Hz input?

EXPERIMENT NO: 04

To Construct and Test a Regulated +5V DC Power Supply

1. Aim

To construct a regulated +5V DC power supply using a step-down transformer, bridge rectifier, filter capacitor, and three-terminal voltage regulator IC 7805, and to test its output for line and load regulation.

2. Theory

A regulated DC power supply converts unregulated AC mains supply into a stable, ripple-free DC output suitable for powering electronic circuits. It typically consists of four stages: a step-down transformer to reduce the AC mains voltage to a safe low level, a bridge rectifier to convert the AC into pulsating DC, a filter capacitor to smooth the pulsating DC into a nearly steady DC with some ripple, and a voltage regulator IC to eliminate the remaining ripple and hold the output constant despite variations in input voltage or load current.

The IC 7805 is a member of the 78xx series of three-terminal positive fixed voltage regulators. It accepts an unregulated DC input, typically between 7V and 25V, and provides a fixed regulated output of +5V at currents up to about 1A. Internally it uses a reference voltage source, an error amplifier, and a series pass transistor to continuously compare the output voltage against the reference and adjust the pass transistor to keep the output constant. It also incorporates built-in protection features such as thermal shutdown, current limiting, and safe-operating-area protection.

A small bypass capacitor (typically 0.1µF) is connected at the output of the IC close to its terminals to improve transient response and suppress high-frequency noise.

3. Practical Set-up / Circuit Diagram

Fig 4: Circuit Diagram - Regulated +5V DC Power Supply (using IC 7805)

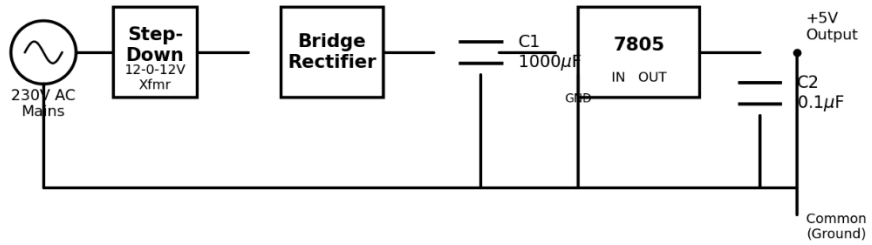

Fig. 4.1: Regulated +5V DC power supply using IC 7805

The 230V AC mains is stepped down by the transformer, rectified by the bridge rectifier, filtered by capacitor C1, and then applied to the input (IN) pin of IC 7805. The regulated +5V output is available at the OUT pin with respect to the common (GND) pin, with bypass capacitor C2 connected at the output.

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	Step-down Transformer	230V/12-0-12V, 1A	1
2	Rectifier Diodes	IN4007	4
3	Voltage Regulator IC	IC 7805	1
4	Filter Capacitor C1	1000µF/25V	1
5	Bypass Capacitor C2	0.1µF (ceramic)	1
6	Digital Multimeter	0-30V DC	1
7	Decade Resistance Box / Load Resistor	Variable / 100Ω-1kΩ	1
8	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Identify the IN, OUT, and GND pins of IC 7805 correctly from its datasheet before connecting.
- Check polarity of the bridge rectifier output and filter capacitor before feeding it to the IC.
- Do not connect the load directly without verifying the circuit; ensure the load current stays within the rated current of the IC.
- Use a heat sink for the IC if it is expected to dissipate significant power for extended durations.
- Do not touch the transformer primary side while mains supply is on.
- Switch off supply before modifying circuit connections.

6. Procedure

- Connect the step-down transformer, bridge rectifier, and filter capacitor C1 as shown in Fig. 4.1.
- Connect the IC 7805 with its input pin to the filtered DC and ground pin to circuit common.
- Connect the bypass capacitor C2 between the output and ground pins of the IC.
- Switch on the AC mains supply and measure the unregulated DC voltage at the input of the IC using a multimeter.
- Measure the regulated DC output voltage at the OUT pin; it should read close to +5V.
- Vary the input AC voltage slightly (if a variac is available) and note whether the output remains constant (line regulation).
- Connect a variable load resistor at the output and vary the load current, noting the output voltage at each step (load regulation).

7. Observations and Calculations (Observations Table)

S.No.	Unregulated Input (V)	Load Current (mA)	Regulated Output (V)	% Regulation
1				
2				
3				
4				

Calculations: % Load Regulation = [(Vno-load − Vfull-load) / Vfull-load] × 100.

8. Results

A regulated +5V DC power supply was successfully constructed using IC 7805. The output voltage was measured to remain close to +5V for variations in the unregulated input voltage and for varying load current, confirming satisfactory line and load regulation of the power supply.

9. Viva Book

1. What are the three terminals of IC 7805 and their functions?
2. What is the minimum input-output voltage difference (dropout voltage) required for the 7805 to regulate properly?
3. What is the maximum output current rating of IC 7805?
4. Why is a heat sink sometimes required with the 7805?
5. Differentiate between line regulation and load regulation.
6. What is the purpose of the bypass capacitor at the output of the regulator IC?

EXPERIMENT NO: 05

To Construct and Test a Regulated -5V DC Power Supply

1. Aim

To construct a regulated -5V DC power supply using a step-down transformer, bridge rectifier, filter capacitor, and three-terminal negative voltage regulator IC 7905, and to test its output for line and load regulation.

2. Theory

The IC 7905 belongs to the 79xx series of three-terminal negative fixed voltage regulators and is the negative-voltage counterpart of the 78xx series. It accepts a negative unregulated DC input voltage and delivers a fixed regulated output of -5V with respect to common ground, at currents up to about 1A. The internal structure and working principle are similar to the 7805 — an internal reference, error amplifier, and series-pass element continuously regulate the output — except that the polarities of all internal stages are reversed to handle negative voltages.

To generate the required negative unregulated DC input, the circuit uses the same step-down transformer and bridge rectifier arrangement as a positive supply, but the output polarity taken from the bridge is reversed (i.e., the terminal that would normally be the negative/ground terminal for a positive supply is instead treated as the input, and the other terminal is treated as common), so that a negative voltage with respect to common is presented to the IN pin of the 7905.

Such negative supplies are commonly required alongside a +5V supply to provide dual (±5V) rails needed by operational amplifiers, comparators, and certain analog and interface ICs (e.g., RS-232 line drivers).

3. Practical Set-up / Circuit Diagram

Fig 5: Circuit Diagram - Regulated -5V DC Power Supply (using IC 7905)

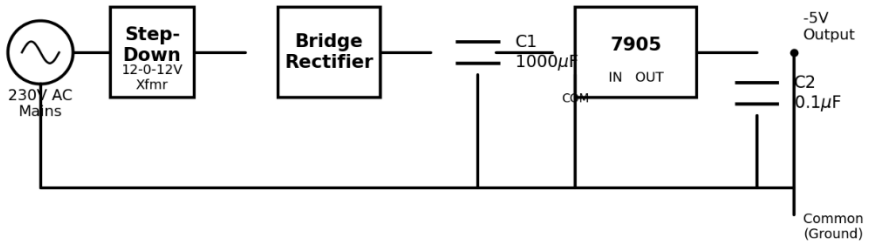

Fig. 5.1: Regulated -5V DC power supply using IC 7905

The step-down transformer output is rectified using a bridge rectifier and filtered by capacitor C1, with the polarity arranged so that a negative unregulated voltage (with respect to common) is applied to the IN pin of IC 7905. The regulated -5V output is obtained at the OUT pin, with bypass capacitor C2 connected at the output for stability.

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	Step-down Transformer	230V/12-0-12V, 1A	1
2	Rectifier Diodes	IN4007	4
3	Voltage Regulator IC	IC 7905	1
4	Filter Capacitor C1	1000µF/25V	1
5	Bypass Capacitor C2	0.1µF (ceramic)	1
6	Digital Multimeter	0-30V DC	1
7	Decade Resistance Box / Load Resistor	Variable / 100Ω-1kΩ	1
8	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Identify the IN, OUT, and common (GND) pins of IC 7905 correctly from its datasheet — pin configuration differs from the 78xx series.
- Ensure the correct polarity of the rectified/filtered DC is applied to the IC input; reversed polarity will damage the IC.
- Do not exceed the rated output current of the IC when connecting the load.
- Use a heat sink for the IC for extended operation at higher currents.
- Do not touch the transformer primary side while mains supply is switched on.
- Switch off the supply before modifying any circuit connections.

6. Procedure

- Connect the step-down transformer, bridge rectifier, and filter capacitor C1 as shown in Fig. 5.1, ensuring the correct negative polarity is presented to the IC input.
- Connect the IC 7905 with its input pin to the negative filtered DC and its common pin to circuit ground.
- Connect the bypass capacitor C2 between the output and common pins of the IC.
- Switch on the AC supply and measure the unregulated DC input voltage to the IC using a multimeter.
- Measure the regulated DC output voltage at the OUT pin with respect to common; it should read close to -5V.
- Vary the input AC voltage slightly, if possible, and note whether the output remains constant (line regulation).
- Connect a variable load at the output and vary the load current, noting the output voltage at each step (load regulation).

7. Observations and Calculations (Observations Table)

S.No.	Unregulated Input (V)	Load Current (mA)	Regulated Output (V)	% Regulation
1				
2				
3				
4				

Calculations: % Load Regulation = [(Vno-load − Vfull-load) / Vfull-load] × 100 (magnitudes used for negative voltage).

8. Results

A regulated -5V DC power supply was successfully constructed using IC 7905. The output voltage was measured to remain close to -5V for variations in the unregulated input voltage and for varying load current, confirming satisfactory line and load regulation of the negative power supply.

9. Viva Book

1. How does the IC 7905 differ from the IC 7805 in terms of pin configuration and polarity?
2. Why is a negative supply required in many analog circuits?
3. What precautions are necessary when handling negative voltage regulator circuits?
4. What is the effect of reversing input polarity to a 79xx series regulator?
5. How can a dual ±5V supply be derived using 7805 and 7905 together?
6. What is the significance of the bypass capacitor at the input and output of the regulator IC?

EXPERIMENT NO: 06

Identify the Given Transistor (Terminal Identification and Type Test)

1. Aim

To identify the terminals (Base, Emitter, Collector) and the type (NPN or PNP) of a given unmarked/unknown transistor using a digital multimeter.

2. Theory

A bipolar junction transistor (BJT) consists of two p-n junctions formed by three doped regions — Emitter, Base and Collector — arranged as either NPN or PNP. Each of the two junctions (Base-Emitter and Base-Collector) behaves like an ordinary diode. This diode-like behaviour of the junctions can be exploited to identify the terminals and type of an unknown transistor using a multimeter set to diode-check (or resistance) mode.

In an NPN transistor, the Base is the common terminal (P-type) to which both the Emitter and Collector (both N-type) junctions show forward conduction when the red (positive) probe is placed on the Base. In a PNP transistor, the Base is the common terminal (N-type) and forward conduction (a low reading / diode drop of about 0.6-0.7V) is obtained when the black (negative) probe is placed on the Base, since the P-regions (Emitter/Collector) must be at higher potential relative to the N-type Base for forward conduction. The terminal that shows forward drop with both other terminals is the Base; the transistor type is identified from whether the red or black probe was on the Base for conduction. The Emitter and Collector are further distinguished because the Emitter-Base junction is more heavily doped than the Collector-Base junction, giving a slightly lower forward voltage drop reading (or a gain/hFE test on a transistor tester can be used to confirm).

3. Practical Set-up / Circuit Diagram

Fig. 1.1: Transistor terminal identification using multimeter (diode mode)

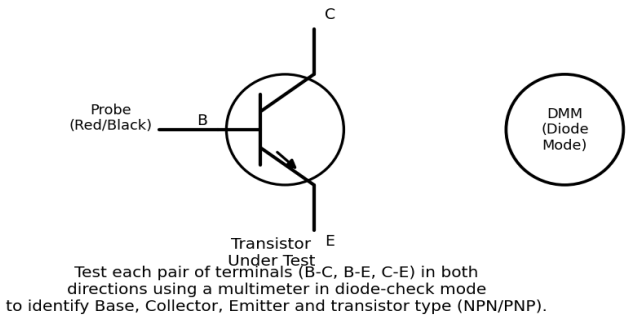

Fig. 1.1: Transistor terminal identification using a multimeter in diode-check mode

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	Transistor (unknown/unmarked)	BC547/BC557 type	1
2	Digital Multimeter (DMM)	With diode-check mode	1
3	Transistor Socket / Breadboard	Standard	1

5. Precautions to be Followed

- Handle the transistor carefully; avoid excessive heat or static discharge while testing.
- Set the multimeter correctly to diode-check (or resistance) mode before testing.
- Note the reading carefully for each of the six probe combinations (3 pairs x 2 polarities).
- Do not apply external power supply directly across the junctions during this test.
- Record observations systematically to avoid confusion between Emitter and Collector.

6. Procedure

- Set the digital multimeter to diode-check mode.
- Label the three terminals of the transistor as 1, 2 and 3 (arbitrary, since unknown).
- Place the red probe on terminal 1 and black probe on terminal 2; note the reading. Repeat for all 6 possible probe combinations among the three terminals.
- Identify the terminal which shows a forward diode-drop reading (approx. 0.6-0.7V) with both of the other two terminals - this is the Base.
- If forward conduction occurs with the red probe on the Base (relative to the other two), the transistor is NPN; if it occurs with the black probe on the Base, the transistor is PNP.
- Distinguish Emitter and Collector by comparing the two forward-drop readings from the Base (Emitter-Base junction typically shows a marginally higher/sharper drop) or by using the hFE socket of the multimeter, if available, to confirm the pin arrangement.
- Record the complete pin identification (Base, Emitter, Collector) and the transistor type.

7. Observations and Calculations (Observations Table)

S.No.	Probe Combination (Red-Black)	Meter Reading	Forward/Reverse	Remarks
1	1-2			
2	2-1			
3	1-3			
4	3-1			
5	2-3			
6	3-2			

Result of identification: Base = ___, Emitter = ___, Collector = ___, Transistor Type = NPN / PNP (strike out one).

8. Results

The given transistor was tested using the diode-check method on a digital multimeter, and its Base, Emitter and Collector terminals were successfully identified. The transistor was determined to be of NPN / PNP type based on the polarity of forward conduction observed.

9. Viva Book

1. What is the working principle of the diode-check method for transistor identification?
2. How can you distinguish an NPN transistor from a PNP transistor using a multimeter?
3. Why is the Emitter-Base junction more heavily doped than the Collector-Base junction?
4. What is hFE and how is it measured?
5. Why can't an ohmmeter with reversed internal battery polarity give reliable diode-mode readings?

EXPERIMENT NO: 07

Test the Input and Output Characteristics of the CE Amplifier

1. Aim

To plot the input characteristics (VBE vs IB) and output characteristics (VCE vs IC) of a transistor connected in Common Emitter (CE) configuration.

2. Theory

In the Common Emitter (CE) configuration, the emitter terminal is common to both the input (base-emitter) and output (collector-emitter) circuits. The input characteristic is a plot of base current (IB) versus base-emitter voltage (VBE) for a constant collector-emitter voltage (VCE), and it resembles the forward characteristic of a p-n junction diode. The output characteristic is a family of curves plotting collector current (IC) versus VCE for different constant values of IB, showing three regions of operation: the cut-off region (IB = 0, IC almost 0), the active region (IC nearly constant with VCE, controlled by IB - used for amplification), and the saturation region (small VCE, IC rises steeply with VCE).

The CE configuration provides both current gain and voltage gain, along with a 180-degree phase reversal between input and output, and is therefore the most commonly used configuration for amplification.

3. Practical Set-up / Circuit Diagram

Fig. 2.1: CE Amplifier - Voltage Divider Bias Circuit

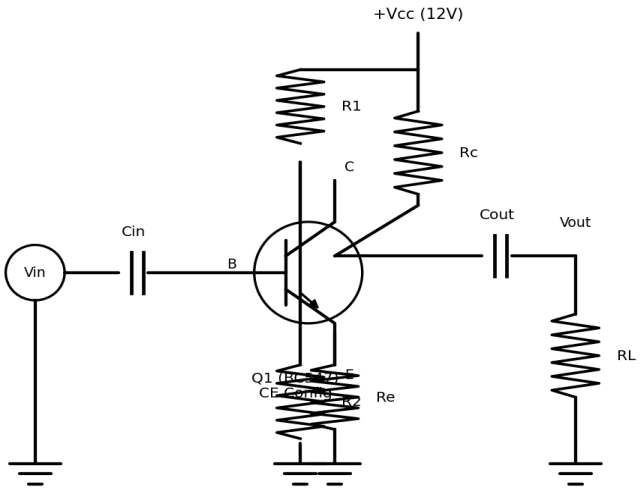

Fig. 2.1: CE Configuration test circuit (double power supply method - VBB for base bias, VCC for collector)

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	NPN Transistor	BC547	1
2	Regulated Power Supplies (two)	0-1V and 0-15V DC	2
3	Resistors	1k-ohm / 10k-ohm	2
4	Voltmeters	0-1V and 0-15V DC	2
5	Micro-ammeter	0-500uA	1
6	Milliammeter	0-30mA	1
7	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Ensure correct polarity of the transistor and both DC supplies before switching on.
- Increase supply voltages gradually; do not exceed the maximum ratings of the transistor.
- Keep VCE constant while varying IB for input characteristics, and vice versa for output characteristics.
- Avoid parallax error while noting meter readings.
- Do not leave the transistor biased at high current for long periods to prevent heating.

6. Procedure

Input Characteristics

- Connect the circuit as shown in Fig. 2.1.
- Keep VCE constant at a fixed value (e.g., 5V) using the collector supply.
- Vary the base supply VBB in small steps and note the corresponding VBE and IB readings.
- Repeat for another fixed value of VCE (e.g., 10V) and tabulate readings separately.
- Plot IB (Y-axis) versus VBE (X-axis) for each value of VCE.

Output Characteristics

- Set the base current IB to a fixed value (e.g., 20uA) using the base supply.
- Vary the collector supply VCC in steps and note VCE and the corresponding IC.
- Repeat for other fixed values of IB (e.g., 40uA, 60uA).
- Plot IC (Y-axis) versus VCE (X-axis) for each value of IB to obtain the output characteristic family.

7. Observations and Calculations (Observations Table)

Input Characteristics (VCE = constant)

S.No.	VBE (V)	IB (uA)	VCE (constant) (V)
1			
2			
3			
4			

Output Characteristics (IB = constant)

S.No.	VCE (V)	IC (mA)	IB (constant) (uA)
1			
2			
3			
4			

8. Results

The input and output characteristics of the transistor in CE configuration were plotted successfully. The input characteristic showed a diode-like exponential curve, and the output characteristic showed distinct cut-off, active and saturation regions, confirming the expected behaviour of a CE amplifier.

9. Viva Book

1. Why is CE configuration most commonly used for amplification?
2. What are the three regions of operation visible in the output characteristics?
3. Define input resistance and output resistance from the CE characteristics.
4. Why does the collector current remain nearly constant in the active region despite increasing VCE?
5. What is the phase relationship between input and output in a CE amplifier?

EXPERIMENT NO: 08

Test the Input and Output Characteristics of the CC Amplifier

1. Aim

To plot the input characteristics (VBC vs IB) and output characteristics (VEC vs IE) of a transistor connected in Common Collector (CC) configuration.

2. Theory

In the Common Collector (CC) configuration, also known as the emitter follower, the collector terminal is common to both input and output circuits, the input signal is applied between base and collector, and the output is taken between emitter and collector. The input characteristic is a plot of IB versus VBC for a constant VEC, while the output characteristic is a plot of IE versus VEC for different constant values of IB.

The CC configuration provides a voltage gain of nearly (but always less than) unity, a high current gain, high input impedance and low output impedance, with no phase reversal between input and output. Because of these properties it is primarily used as a buffer or impedance-matching stage rather than for voltage amplification.

3. Practical Set-up / Circuit Diagram

Fig. 3.1: CC Amplifier (Emitter Follower) Circuit

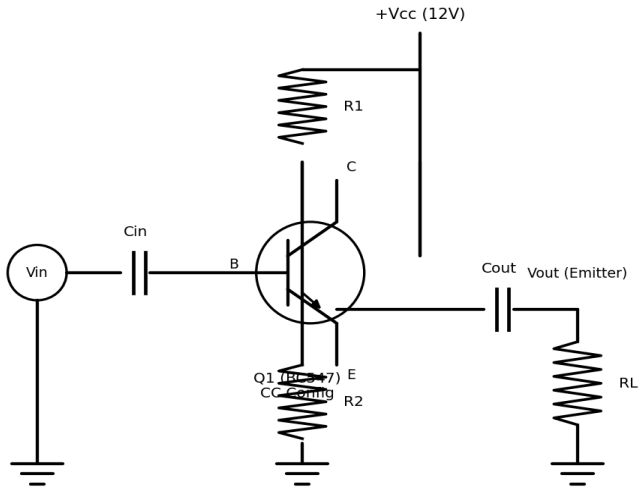

Fig. 3.1: CC Configuration (Emitter Follower) test circuit

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	NPN Transistor	BC547	1
2	Regulated Power Supplies (two)	0-1V and 0-15V DC	2
3	Resistors	1k-ohm / 10k-ohm	2
4	Voltmeters	0-1V and 0-15V DC	2
5	Micro-ammeter	0-500uA	1
6	Milliammeter	0-30mA	1
7	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Ensure correct polarity of transistor and supplies before switching on.
- Vary the supply voltages gradually and within the transistor's safe operating limits.
- Keep VEC constant while varying IB for input characteristics, and vice versa for output characteristics.
- Take care to note the emitter current accurately since it is the output parameter of interest here.
- Avoid loose connections on the breadboard.

6. Procedure

Input Characteristics

- Connect the circuit as shown in Fig. 3.1.
- Keep VEC constant at a fixed value using the collector supply.
- Vary the base-collector bias and note the corresponding VBC and IB readings.
- Repeat for another fixed value of VEC and tabulate readings separately.
- Plot IB (Y-axis) versus VBC (X-axis) for each value of VEC.

Output Characteristics

- Set the base current IB to a fixed value.
- Vary VEC in steps and note the corresponding emitter current IE.
- Repeat for other fixed values of IB.
- Plot IE (Y-axis) versus VEC (X-axis) for each value of IB.

7. Observations and Calculations (Observations Table)

Input Characteristics (VEC = constant)

S.No.	VBC (V)	IB (uA)	VEC (constant) (V)
1			
2			
3			
4			

Output Characteristics (IB = constant)

S.No.	VEC (V)	IE (mA)	IB (constant) (uA)
1			
2			
3			
4			

8. Results

The input and output characteristics of the transistor in CC configuration were plotted. The output characteristic confirmed that IE is approximately equal to IC and remains nearly independent of VEC in the active region, while the CC stage exhibited near-unity voltage gain, consistent with emitter-follower behaviour.

9. Viva Book

1. Why is the CC configuration called an emitter follower?
2. What is the typical voltage gain of a CC amplifier and why?
3. Why does CC configuration have high input impedance and low output impedance?
4. Where is the CC configuration typically used in practical circuits?
5. What is the phase relationship between input and output in a CC amplifier?

EXPERIMENT NO: 09

Test the Input and Output Characteristics of the CB Amplifier

1. Aim

To plot the input characteristics (VEB vs IE) and output characteristics (VCB vs IC) of a transistor connected in Common Base (CB) configuration.

2. Theory

In the Common Base (CB) configuration, the base terminal is common to both input (emitter-base) and output (collector-base) circuits. The input characteristic is a plot of emitter current IE versus emitter-base voltage VEB for a constant collector-base voltage VCB, and closely resembles a forward diode characteristic. The output characteristic is a plot of collector current IC versus VCB for different fixed values of IE, and shows that IC remains almost constant and nearly equal to IE over a wide range of VCB - indicating a very high output resistance.

The CB configuration provides a current gain (alpha, a) slightly less than unity, a high voltage gain, low input impedance, very high output impedance, and no phase reversal between input and output. Because of its excellent high-frequency response, it is mainly used in high-frequency and RF amplifier applications.

3. Practical Set-up / Circuit Diagram

Fig. 4.1: CB Amplifier Circuit

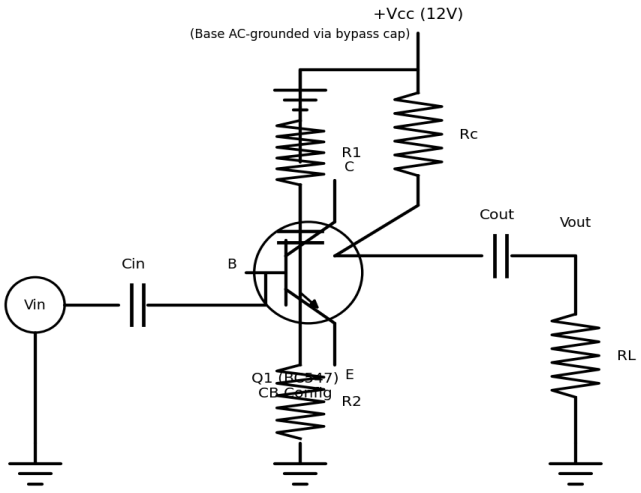

Fig. 4.1: CB Configuration test circuit

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	NPN Transistor	BC547	1
2	Regulated Power Supplies (two)	0-1V and 0-15V DC	2
3	Resistors	1k-ohm / 10k-ohm	2
4	Voltmeters	0-1V and 0-15V DC	2
5	Milliammeters	0-30mA (two)	2
6	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Ensure correct polarity of transistor and both DC supplies before switching on.
- Increase supply voltages gradually within the transistor's safe operating range.
- Keep VCB constant while varying IE for input characteristics, and vice versa for output characteristics.
- Ensure the base terminal is properly AC/DC grounded as required by the CB configuration.
- Avoid loose or reversed meter connections.

6. Procedure

Input Characteristics

- Connect the circuit as shown in Fig. 4.1.
- Keep VCB constant at a fixed value using the collector supply.
- Vary the emitter-base bias in steps and note the corresponding VEB and IE readings.
- Repeat for another fixed value of VCB and tabulate readings separately.
- Plot IE (Y-axis) versus VEB (X-axis) for each value of VCB.

Output Characteristics

- Set IE to a fixed value using the emitter supply.
- Vary VCB in steps and note the corresponding IC.
- Repeat for other fixed values of IE.
- Plot IC (Y-axis) versus VCB (X-axis) for each value of IE.

7. Observations and Calculations (Observations Table)

Input Characteristics (VCB = constant)

S.No.	VEB (V)	IE (mA)	VCB (constant) (V)
1			
2			
3			
4			

Output Characteristics (IE = constant)

S.No.	VCB (V)	IC (mA)	IE (constant) (mA)
1			
2			
3			
4			

8. Results

The input and output characteristics of the transistor in CB configuration were plotted. The output characteristic confirmed that IC is almost equal to and nearly independent of IE over a wide range of VCB, indicating a current gain (alpha) close to but less than unity and a very high output resistance.

9. Viva Book

1. Define alpha of a transistor in CB configuration.
2. Why does the CB configuration have low input impedance?
3. Why is CB configuration preferred for high-frequency applications?
4. What is the relationship between alpha and beta of a transistor?
5. What is the phase relationship between input and output in a CB amplifier?

EXPERIMENT NO: 10

Measure the Voltage Gain and Current Gain of CE Configuration

1. Aim

To measure the voltage gain (Av) and current gain (Ai) of a single-stage transistor amplifier in Common Emitter (CE) configuration, and to observe the input-output phase relationship.

2. Theory

A CE amplifier is built using a transistor biased in its active region (commonly using voltage-divider bias for stability), with the emitter terminal common to the input and output loops. A small AC signal applied at the base, after being coupled through an input capacitor, produces an amplified and phase-inverted (180-degree shifted) AC signal at the collector, coupled to the load through an output capacitor. The voltage gain is defined as Av = Vout/Vin and can be calculated theoretically as Av is approximately -Rc/re, where Rc is the collector resistor and re is the small-signal emitter resistance.

The current gain of the CE stage is closely related to the transistor's forward current transfer ratio, beta (hFE) = IC/IB, and represents how effectively the base current controls a much larger collector current. Practically, Av and Ai are measured by observing input and output signal amplitudes on a CRO or by using AC millivoltmeters, and comparing the measured values with the theoretical estimates obtained from the biasing resistor values and the transistor's small-signal parameters.

3. Practical Set-up / Circuit Diagram

Fig. 2.1: CE Amplifier - Voltage Divider Bias Circuit

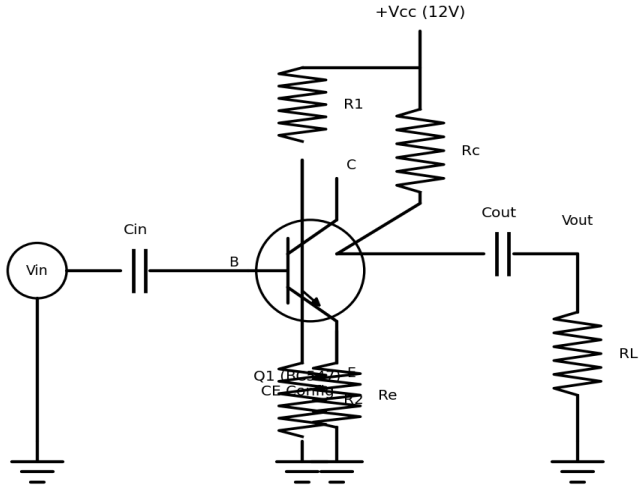

Fig. 5.1: CE Amplifier circuit for voltage and current gain measurement (same as Fig. 2.1)

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	NPN Transistor	BC547	1
2	Resistors (R1, R2, Rc, Re, RL)	As per design	5
3	Coupling/Bypass Capacitors	10uF/100uF	3
4	Function Generator	0-1MHz, sine wave	1
5	Dual Trace CRO	20-30 MHz	1
6	Regulated DC Power Supply	0-15V	1
7	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Keep the input signal amplitude small enough to avoid clipping/distortion at the output.
- Verify correct DC bias point (Q-point) before applying the AC input signal.
- Use proper grounding common to the function generator, CRO and circuit.
- Select an appropriate input signal frequency within the amplifier's mid-band region.
- Check CRO probe compensation and volts/division settings before measurement.

6. Procedure

- Connect the CE amplifier circuit as shown in Fig. 5.1 and verify the DC operating point (VCE, IC) without input signal.
- Apply a small sinusoidal AC input signal (e.g., 1kHz, few mV) from the function generator.
- Observe the input and output waveforms simultaneously on the dual-trace CRO; verify the 180-degree phase inversion.
- Measure the peak-to-peak amplitude of the input signal (Vin) and output signal (Vout).
- Calculate the voltage gain: Av = Vout / Vin.
- Using the DC bias readings (IB and IC), determine the current gain: Ai is approximately beta = IC/IB.
- Repeat measurement at a couple of different input frequencies to verify the gain remains fairly constant in the mid-band.

7. Observations and Calculations (Observations Table)

S.No.	Frequency (Hz)	Vin (p-p) (V)	Vout (p-p) (V)	Voltage Gain Av	Phase Shift
1					
2					
3					

Calculations: Av = Vout/Vin; Ai is approximately beta = IC(DC)/IB(DC); Power Gain Ap = Av x Ai.

8. Results

The voltage gain and current gain of the CE amplifier were measured. The output was found to be an amplified and 180-degree phase-inverted version of the input, confirming the characteristic high voltage gain, high current gain, and phase reversal of the CE configuration.

Viva Book

1. Why does the CE amplifier provide both voltage gain and current gain?
2. Why is there a 180-degree phase shift between input and output in a CE amplifier?
3. What is the significance of the emitter bypass capacitor on the gain?
4. How does the value of Rc affect the voltage gain of a CE amplifier?
5. What causes gain roll-off at very high or very low frequencies?

EXPERIMENT NO: 11

Measure the Voltage Gain and Current Gain of CC Configuration

1. Aim

To measure the voltage gain (Av) and current gain (Ai) of a single-stage transistor amplifier in Common Collector (CC) configuration.

2. Theory

The CC (emitter-follower) amplifier has its output taken across the emitter resistor, with the collector directly connected to the DC supply (AC ground). Because of 100% negative feedback (the entire output is fed back in series with the input), the voltage gain of a CC amplifier is always slightly less than unity (Av approximately 1), and there is no phase reversal between input and output - the output follows the input in phase, hence the name 'emitter follower'.

Despite the near-unity voltage gain, the CC amplifier provides a large current gain, approximately equal to (beta+1), since the emitter current is the sum of the base and collector currents. Combined with its high input impedance and low output impedance, this makes the CC stage extremely useful as a buffer amplifier for impedance matching between a high-impedance source and a low-impedance load, without significant loss of signal amplitude.

3. Practical Set-up / Circuit Diagram

Fig. 3.1: CC Amplifier (Emitter Follower) Circuit

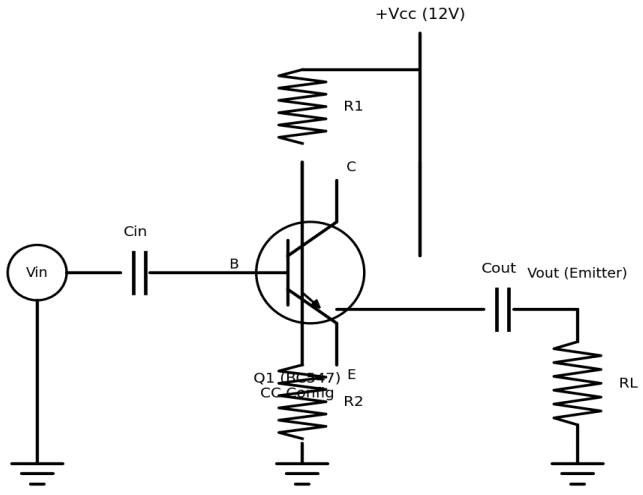

Fig. 6.1: CC Amplifier (Emitter Follower) circuit for gain measurement (same as Fig. 3.1)

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	NPN Transistor	BC547	1
2	Resistors (R1, R2, RE, RL)	As per design	4
3	Coupling Capacitors	10uF	2
4	Function Generator	0-1MHz, sine wave	1
5	Dual Trace CRO	20-30 MHz	1
6	Regulated DC Power Supply	0-15V	1
7	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Keep the input signal amplitude within the linear range of operation to avoid distortion.
- Verify the DC bias point before applying the AC input.
- Ensure common ground reference between generator, CRO and circuit.
- Check for correct probe compensation on the CRO before taking amplitude readings.
- Avoid loading the output excessively, which can reduce the effective gain.

6. Procedure

- Connect the CC amplifier circuit as shown in Fig. 6.1 and verify the DC bias conditions.
- Apply a small sinusoidal AC input signal (e.g., 1kHz) from the function generator.
- Observe input and output waveforms on the dual-trace CRO and verify there is no phase reversal.
- Measure the peak-to-peak input voltage (Vin) and output voltage (Vout) across RL (emitter).
- Calculate the voltage gain: Av = Vout/Vin (expect a value close to but less than 1).
- Determine current gain: Ai is approximately (beta+1) using the DC bias readings of IB and IE.
- Repeat at a different signal frequency to confirm consistency of the measured gain.

7. Observations and Calculations (Observations Table)

S.No.	Frequency (Hz)	Vin (p-p) (V)	Vout (p-p) (V)	Voltage Gain Av	Phase Shift
1					
2					
3					

Calculations: Av = Vout/Vin (approximately 1); Ai is approximately (beta+1) = IE(DC)/IB(DC); Power Gain Ap = Av x Ai.

8. Results

The voltage gain and current gain of the CC amplifier were measured. The voltage gain was found to be close to unity with no phase reversal, while the current gain was found to be high (approximately beta+1), confirming the emitter-follower / buffer characteristics of the CC configuration.

9. Viva Book

1. Why is the voltage gain of a CC amplifier always less than unity?
2. Why is there no phase reversal in a CC amplifier?
3. Derive the approximate expression for current gain of a CC amplifier.
4. Where is a CC (emitter follower) stage typically used in a multistage amplifier?
5. Why does the CC amplifier have high input impedance and low output impedance?

EXPERIMENT NO: 12

Measure the Voltage Gain and Current Gain of CB Configuration

1. Aim

To measure the voltage gain (Av) and current gain (Ai) of a single-stage transistor amplifier in Common Base (CB) configuration.

2. Theory

In a CB amplifier, the input signal is applied at the emitter and the output is taken from the collector, with the base held at AC ground (common). The current gain of the CB configuration, denoted alpha, is defined as Ai = IC/IE and is always slightly less than unity, since IC is always marginally smaller than IE due to a small recombination/base current. Despite this less-than-unity current gain, the CB amplifier can provide a very high voltage gain because the output resistance (collector side) is very much larger than the input resistance (emitter side), so Av = Ai x (Rout/Rin) can still be large.

The CB amplifier has no phase reversal between input and output. Because of its low input impedance, high output impedance, high voltage gain and excellent frequency response, it is often used in high-frequency applications such as RF amplifiers and impedance-matching stages from a low-impedance source to a high-impedance load.

3. Practical Set-up / Circuit Diagram

Fig. 4.1: CB Amplifier Circuit

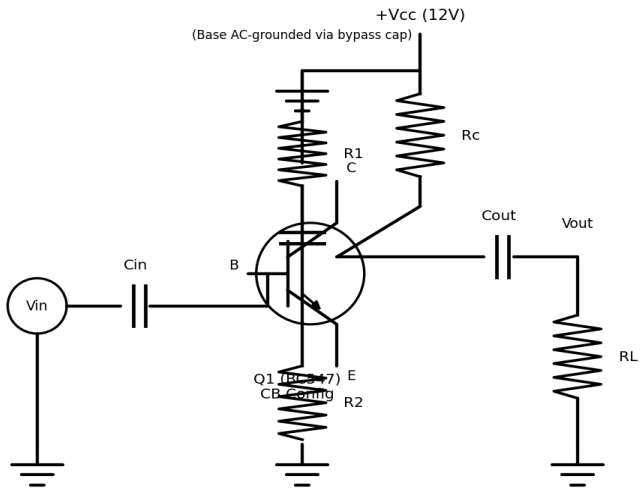

Fig. 7.1: CB Amplifier circuit for gain measurement (same as Fig. 4.1)

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	NPN Transistor	BC547	1
2	Resistors (R1, R2, Rc, RL)	As per design	4
3	Coupling/Bypass Capacitors	10uF/100uF	3
4	Function Generator	0-1MHz, sine wave	1
5	Dual Trace CRO	20-30 MHz	1
6	Regulated DC Power Supply	0-15V	1
7	Breadboard & Connecting Wires	Standard	As required

5. Precautions to be Followed

- Ensure the base terminal is properly bypassed to AC ground before applying signal.
- Keep the input signal amplitude small to avoid distortion at the output.
- Verify DC bias conditions before applying the AC input signal.
- Ensure common ground reference between the function generator, CRO and circuit.
- Check CRO probe compensation and volts/division settings before measurement.

6. Procedure

- Connect the CB amplifier circuit as shown in Fig. 7.1 and verify the DC bias point.
- Apply a small sinusoidal AC input signal at the emitter from the function generator.
- Observe input and output waveforms on the dual-trace CRO and confirm there is no phase reversal.
- Measure the peak-to-peak input voltage (Vin) and output voltage (Vout).
- Calculate the voltage gain: Av = Vout/Vin.
- Using DC bias readings of IE and IC, determine current gain: Ai (alpha) = IC/IE.
- Repeat measurement at a different frequency and verify the gain remains fairly constant over the mid-band.

7. Observations and Calculations (Observations Table)

S.No.	Frequency (Hz)	Vin (p-p) (V)	Vout (p-p) (V)	Voltage Gain Av	Phase Shift
1					
2					
3					

Calculations: Av = Vout/Vin; Ai (alpha) = IC(DC)/IE(DC) (slightly less than 1); Power Gain Ap = Av x Ai.

8. Results

The voltage gain and current gain of the CB amplifier were measured. The current gain (alpha) was found to be slightly less than unity, while the voltage gain was found to be high, with no phase reversal between input and output, confirming the characteristic behaviour of the CB configuration.

9. Viva Book

1. Why is the current gain of a CB amplifier always less than unity?
2. How can a CB amplifier still provide a high voltage gain despite Ai < 1?
3. Why is there no phase reversal in a CB amplifier?
4. Why is CB configuration suitable for RF/high-frequency applications?
5. Compare the input and output impedance of CB configuration with CE and CC configurations.

EXPERIMENT NO: 13

Test the Functionality of Given Logic Gates using ICs

1. Aim

To study and verify the truth tables of basic logic gates - AND, OR, NOT, NAND, NOR, XOR and XNOR - using their respective ICs.

2. Theory

A logic gate is a digital circuit that performs a specific Boolean logic operation on one or more binary inputs to produce a single binary output. The AND gate (IC 7408) gives output 1 only when all inputs are 1. The OR gate (IC 7432) gives output 1 when at least one input is 1. The NOT gate (IC 7404) is an inverter, producing the complement of the input. The NAND gate (IC 7400) and NOR gate (IC 7402) are the complements of AND and OR respectively, and are called universal gates because any other logic gate can be constructed using only NAND gates or only NOR gates. The XOR gate (IC 7486) gives output 1 when the inputs are different, and the XNOR gate gives output 1 when the inputs are the same.

Each of these gates is available as a standard 14-pin DIP TTL/CMOS IC (e.g., 7408 quad 2-input AND, 7432 quad 2-input OR, 7404 hex inverter, 7400 quad 2-input NAND, 7402 quad 2-input NOR, 7486 quad 2-input XOR), with the supply (Vcc) typically at pin 14 and ground at pin 7. The functionality of each gate is verified practically by applying all possible combinations of logic 0 (0V) and logic 1 (+5V) to the inputs and observing the output using an LED indicator or a logic probe/multimeter, and comparing the observed output with the standard truth table.

3. Practical Set-up / Circuit Diagram

Fig. 8.1: General test set-up for verifying logic gate IC truth table

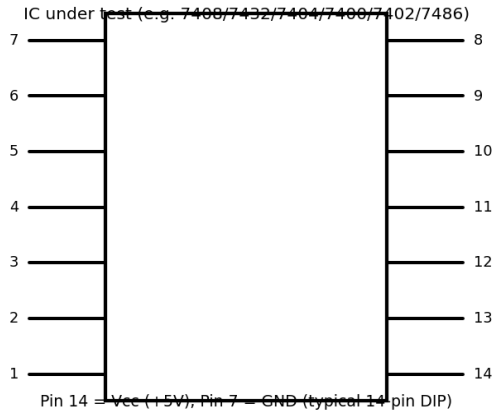

Fig. 8.1: General test set-up for verifying a logic gate IC's truth table

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7408 (AND)	14-pin DIP	1
2	IC 7432 (OR)	14-pin DIP	1
3	IC 7404 (NOT)	14-pin DIP	1
4	IC 7400 (NAND)	14-pin DIP	1
5	IC 7402 (NOR)	14-pin DIP	1
6	IC 7486 (XOR)	14-pin DIP	1
7	Digital IC Trainer Kit / Breadboard	with +5V supply, LEDs, switches	1
8	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Check the IC pin diagram carefully before making connections; identify Vcc and GND pins correctly.
- Ensure supply voltage does not exceed the rated 5V (for TTL) for the IC.
- Insert/remove ICs only when the power supply is switched off.
- Avoid short-circuiting the output pin directly to Vcc or ground.
- Handle CMOS ICs (if used) with anti-static precautions.

6. Procedure

- Identify the pin configuration of the given IC from its datasheet/pin diagram.
- Insert the IC in the trainer kit / breadboard and connect Vcc and GND pins correctly.
- Connect the input pins of one gate within the IC to logic switches, and the output pin to an LED indicator.
- Apply all possible combinations of logic 0 and logic 1 to the inputs (00, 01, 10, 11 for a 2-input gate).
- Note the output (LED ON = logic 1, LED OFF = logic 0) for each input combination.
- Tabulate the observed truth table and compare it with the standard truth table of the gate.
- Repeat the above steps for each of the given logic gate ICs.

7. Observations and Calculations (Observations Table)

A	B	AND	OR	NAND	NOR	XOR
0	0					
0	1					
1	0					
1	1					

8. Results

The truth tables of the AND, OR, NOT, NAND, NOR and XOR logic gates were verified practically using their respective ICs, and the observed outputs were found to match the standard truth tables in each case.

9. Viva Book

1. What is a logic gate and what are the basic types of logic gates?
2. Write the truth table and Boolean expression for XOR and XNOR gates.
3. Why are NAND and NOR called universal gates?
4. What is the difference between positive logic and negative logic?
5. What is the significance of the IC pin numbers 7 and 14 in a standard 14-pin TTL IC?

EXPERIMENT NO: 14

Implement Logic Gates using Universal NAND Gate IC

1. Aim

To realise the basic logic gates - NOT, AND and OR - using only two-input NAND gates (IC 7400), and to verify their truth tables.

2. Theory

The NAND gate is called a universal gate because any Boolean logic function, and hence any other logic gate, can be implemented using only NAND gates. A NOT gate can be obtained by connecting both inputs of a NAND gate together (or tying one input to logic 1), since NAND with identical inputs A, A gives (A.A)' = A'. An AND gate can be obtained by following a NAND gate with a NAND-gate-connected-as-NOT, since (A.B)" = A.B. An OR gate can be realised using three NAND gates, based on De Morgan's theorem: A+B = (A'.B')' = NAND(NOT(A), NOT(B)), i.e., invert both inputs using NAND-as-NOT, then feed them to a third NAND gate.

This experiment demonstrates the practical construction of NOT, AND and OR gate functions purely from 2-input NAND gates available within a single 7400 IC (which contains four 2-input NAND gates), and verifies that the resulting truth tables match the standard gates being emulated.

3. Practical Set-up / Circuit Diagram

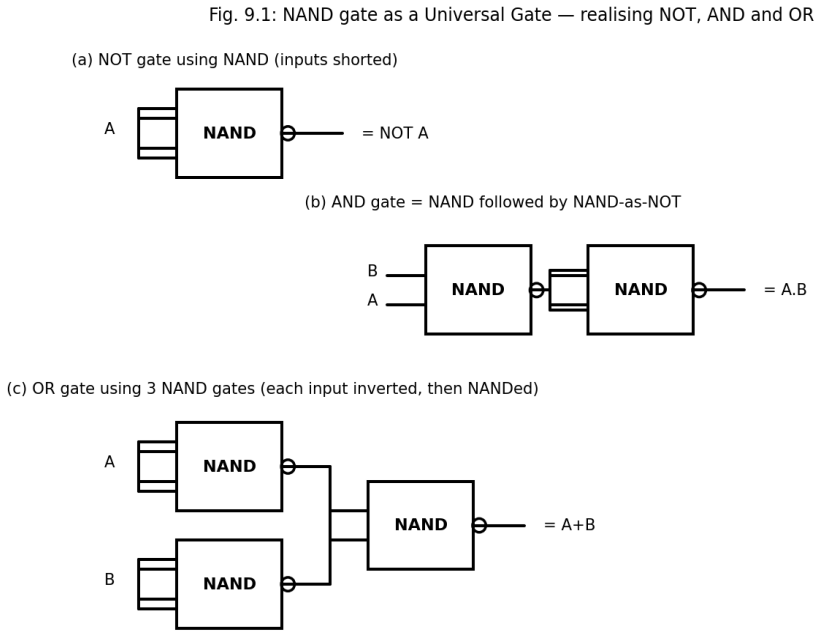

Fig. 9.1: Realisation of NOT, AND and OR gates using NAND gates only

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7400 (Quad 2-input NAND)	14-pin DIP	2
2	Digital IC Trainer Kit / Breadboard	with +5V supply, LEDs, switches	1
3	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Verify the pin diagram of IC 7400 before wiring the individual gates.
- Ensure Vcc and GND connections are made correctly to both ICs (if two are used).
- Do not leave any unused input pins floating; tie them to a fixed logic level as required.
- Double check gate-to-gate interconnections against the logic diagram before switching on.
- Switch off supply before altering connections.

6. Procedure

- Realise a NOT gate by shorting both inputs of one NAND gate together and applying the input signal A; observe the output for A = 0 and A = 1.
- Realise an AND gate by connecting the output of one NAND gate to both inputs of a second NAND gate (as shown in Fig. 9.1(b)); apply all combinations of A and B and note the output.
- Realise an OR gate using three NAND gates as shown in Fig. 9.1(c): invert A and B individually using two NAND-as-NOT gates, then feed these inverted signals into a third NAND gate.
- Apply all four input combinations (00, 01, 10, 11) to each realised gate and record the LED output.
- Compare the observed truth tables with the standard truth tables of NOT, AND and OR gates.

7. Observations and Calculations (Observations Table)

A (NOT test)	Output (NOT)		
0			
1			

A	B	AND (via NAND)	OR (via NAND)	Remarks
0	0			
0	1			
1	0			
1	1			

8. Results

NOT, AND and OR gates were successfully realised using only 2-input NAND gates. The truth tables obtained from the NAND-based circuits matched exactly with the standard truth tables of NOT, AND and OR gates, confirming that NAND is a universal logic gate.

9. Viva Book

1. Prove using Boolean algebra that a NAND gate with shorted inputs acts as a NOT gate.
2. How many NAND gates are minimally required to realise an OR gate?
3. State De Morgan's theorem and its role in universal gate realisation.
4. Why are NAND gates preferred over NOR gates in some IC families?
5. Can an XOR gate be realised using only NAND gates? If so, how many are typically required?

EXPERIMENT NO: 15

Implement Logic Gates using Universal NOR Gate IC

1. Aim

To realise the basic logic gates - NOT, AND and OR - using only two-input NOR gates (IC 7402), and to verify their truth tables.

2. Theory

Like the NAND gate, the NOR gate is also a universal gate, since any Boolean function can be implemented using NOR gates alone. A NOT gate is obtained by shorting both inputs of a NOR gate together, since (A+A)' = A'. An OR gate is obtained by following a NOR gate with a NOR-gate-connected-as-NOT, since (A+B)'' = A+B. An AND gate is realised using three NOR gates, based on De Morgan's theorem: A.B = (A'+B')' = NOR(NOT(A), NOT(B)), i.e., invert both inputs using NOR-as-NOT, then feed them into a third NOR gate.

This experiment practically demonstrates constructing NOT, AND and OR gate functions using only 2-input NOR gates available within the 7402 IC (quad 2-input NOR gate), and verifies that the resulting truth tables match the gates being emulated.

3. Practical Set-up / Circuit Diagram

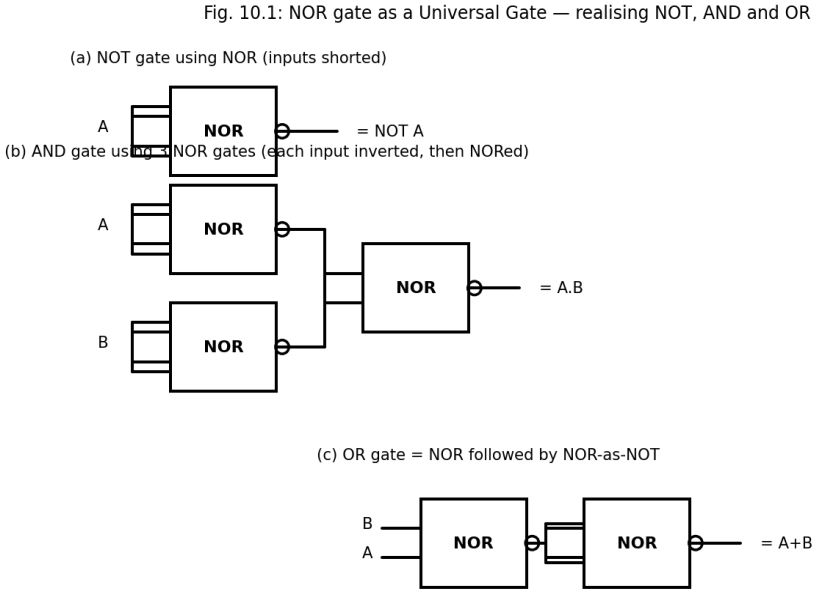

Fig. 10.1: Realisation of NOT, AND and OR gates using NOR gates only

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7402 (Quad 2-input NOR)	14-pin DIP	2
2	Digital IC Trainer Kit / Breadboard	with +5V supply, LEDs, switches	1
3	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Verify the pin diagram of IC 7402 before wiring the individual gates.
- Ensure Vcc and GND connections are made correctly to both ICs (if two are used).
- Do not leave unused input pins floating; tie them to a fixed logic level as required.
- Double check gate interconnections against the logic diagram before switching on the supply.
- Switch off supply before altering any connections.

6. Procedure

- Realise a NOT gate by shorting both inputs of one NOR gate together and applying input A; observe the output for A = 0 and A = 1.
- Realise an AND gate using three NOR gates as shown in Fig. 10.1(b): invert A and B individually using two NOR-as-NOT gates, then feed the inverted signals into a third NOR gate.
- Realise an OR gate by connecting the output of one NOR gate to both inputs of a second NOR gate (as shown in Fig. 10.1(c)).
- Apply all four input combinations (00, 01, 10, 11) to each realised gate and record the LED output.
- Compare the observed truth tables with the standard truth tables of NOT, AND and OR gates.

7. Observations and Calculations (Observations Table)

A (NOT test)	Output (NOT)		
0			
1			

A	B	AND (via NOR)	OR (via NOR)	Remarks
0	0			
0	1			
1	0			
1	1			

8. Results

NOT, AND and OR gates were successfully realised using only 2-input NOR gates. The truth tables obtained from the NOR-based circuits matched exactly with the standard truth tables of NOT, AND and OR gates, confirming that NOR is a universal logic gate.

9. Viva Book

1. Prove using Boolean algebra that a NOR gate with shorted inputs acts as a NOT gate.
2. How many NOR gates are minimally required to realise an AND gate?
3. Compare the practical advantages of using NAND versus NOR as a universal gate.
4. Can a full adder be implemented using only NOR gates? Explain briefly.
5. What do you understand by 'functionally complete' logic gate sets?

EXPERIMENT NO: 16

Implement Half Adder and Half Subtractor using Basic Gates

1. Aim

To design, construct and verify the truth tables of a Half Adder and a Half Subtractor circuit using basic logic gates.

2. Theory

A Half Adder is a combinational logic circuit that adds two single binary digits, A and B, and produces two outputs: SUM and CARRY. The SUM output represents the least significant bit of the addition and is given by the Boolean expression SUM = A XOR B, while the CARRY output (generated when both inputs are 1) is given by CARRY = A.B. A Half Adder can therefore be constructed using one XOR gate (IC 7486) and one AND gate (IC 7408).

A Half Subtractor computes the subtraction of two single bits, A - B, and produces two outputs: DIFFERENCE and BORROW. The difference output is given by DIFF = A XOR B (same as the sum expression), while the borrow output, which is generated when A is 0 and B is 1 (i.e., a larger number is subtracted from a smaller one), is given by BORROW = A'.B, where A' is the complement of A. A Half Subtractor can be constructed using one XOR gate, one NOT gate (IC 7404) and one AND gate.

3. Practical Set-up / Circuit Diagram

Fig. 11.1: Half Adder — SUM = A⊕B, CARRY = A.B

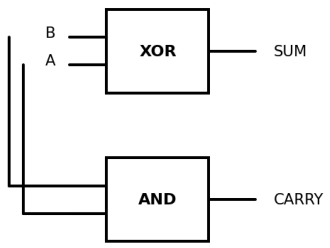

Fig. 11.1: Half Adder logic diagram (SUM = A xor B, CARRY = A.B)

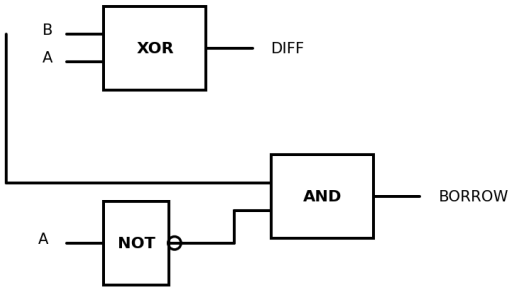

Fig. 11.2: Half Subtractor logic diagram (DIFF = A xor B, BORROW = A'.B)

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7486 (XOR)	14-pin DIP	1
2	IC 7408 (AND)	14-pin DIP	1
3	IC 7404 (NOT)	14-pin DIP	1
4	Digital IC Trainer Kit / Breadboard	with +5V supply, LEDs, switches	1
5	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Verify IC pin diagrams before wiring each gate.
- Ensure correct Vcc/GND connections to all ICs used.
- Cross-check gate interconnections against the logic diagram before applying power.
- Do not leave unused gate inputs floating.
- Switch off the supply before modifying any connection.

6. Procedure

Half Adder

- Connect the XOR gate with inputs A and B to obtain the SUM output, as shown in Fig. 11.1.
- Connect the AND gate with the same inputs A and B to obtain the CARRY output.
- Apply all four combinations of A and B (00, 01, 10, 11) and note SUM and CARRY for each.
- Compare the observed truth table with the standard Half Adder truth table.

Half Subtractor

- Connect the XOR gate with inputs A and B to obtain the DIFF output, as shown in Fig. 11.2.
- Connect a NOT gate to invert input A, and feed A' and B into an AND gate to obtain the BORROW output.
- Apply all four combinations of A and B and note DIFF and BORROW for each.
- Compare the observed truth table with the standard Half Subtractor truth table.

7. Observations and Calculations (Observations Table)

A	B	SUM (A xor B)	CARRY (A.B)	DIFF (A xor B)	BORROW (A'.B)
0	0				
0	1				
1	0				
1	1				

8. Results

The Half Adder and Half Subtractor circuits were constructed using basic logic gates, and their truth tables were verified experimentally. The observed SUM/CARRY and DIFF/BORROW outputs matched the expected theoretical truth tables in all four input combinations.

9. Viva Book

1. Write the Boolean expressions for SUM and CARRY of a Half Adder.
2. Write the Boolean expressions for DIFFERENCE and BORROW of a Half Subtractor.
3. Why is a Half Adder called 'half'? What limitation does it have?
4. Can a Half Adder be converted into a Half Subtractor by adding an inverter? Explain.
5. Draw the truth table of a Half Adder and Half Subtractor from memory.

EXPERIMENT NO: 17

Implement Full Adder using Basic Gates

1. Aim

To design, construct and verify the truth table of a Full Adder circuit using basic logic gates / two Half Adders.

2. Theory

A Full Adder is a combinational circuit that adds three single bits: two significant bits A and B, and a carry input Cin from a previous addition stage, producing two outputs: SUM and carry output Cout. The Boolean expressions are SUM = A xor B xor Cin, and Cout = A.B + Cin.(A xor B), i.e., a carry is generated if any two or more of the three inputs are 1.

A Full Adder can be conveniently constructed using two Half Adder circuits and one OR gate: the first Half Adder adds A and B to produce an intermediate SUM1 and CARRY1; the second Half Adder adds SUM1 and Cin to produce the final SUM and an intermediate CARRY2; the final Cout is obtained by ORing CARRY1 and CARRY2. This modular construction (2 Half Adders + 1 OR gate) is a standard and important building block used in binary adder/subtractor and ALU circuits.

3. Practical Set-up / Circuit Diagram

Fig. 12.1: Full Adder using two Half Adders and an OR gate

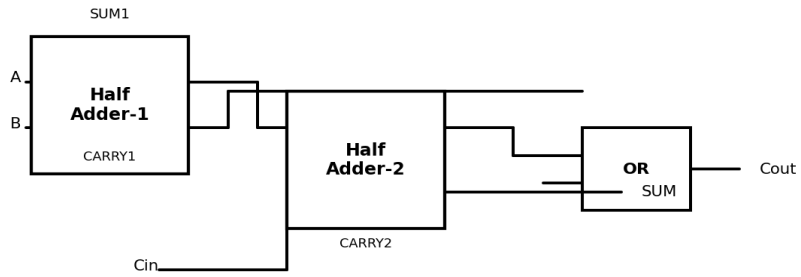

Fig. 12.1: Full Adder realised using two Half Adders and an OR gate

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7486 (XOR)	14-pin DIP	1
2	IC 7408 (AND)	14-pin DIP	1
3	IC 7432 (OR)	14-pin DIP	1
4	Digital IC Trainer Kit / Breadboard	with +5V supply, LEDs, switches	1
5	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Verify IC pin diagrams before wiring each gate stage.
- Ensure correct Vcc/GND connections to all ICs used.
- Cross-check the two Half Adder stages and OR gate wiring against the logic diagram before switching on.
- Do not leave any unused gate inputs floating.
- Switch off supply before modifying any connection.

6. Procedure

- Construct the first Half Adder with inputs A and B, producing SUM1 and CARRY1 (using an XOR and an AND gate).
- Construct the second Half Adder with inputs SUM1 and Cin, producing the final SUM and CARRY2.
- Connect CARRY1 and CARRY2 to the two inputs of an OR gate to obtain Cout.
- Apply all eight combinations of A, B and Cin (000 to 111) and note the SUM and Cout for each.
- Compare the observed truth table with the standard Full Adder truth table.

7. Observations and Calculations (Observations Table)

A	B	Cin	SUM	Cout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

8. Results

The Full Adder circuit was constructed using two Half Adders and an OR gate, and its truth table was verified experimentally for all eight input combinations of A, B and Cin. The observed SUM and Cout outputs matched the standard Full Adder truth table.

9. Viva Book

1. Write the Boolean expressions for SUM and Cout of a Full Adder.
2. How is a Full Adder constructed from two Half Adders?
3. What is the purpose of the carry input Cin in a Full Adder?
4. How can a 4-bit binary adder be constructed using Full Adders?
5. What is the propagation delay significance in a ripple-carry adder made of cascaded Full Adders?

EXPERIMENT NO: 18

Implement Full Subtractor using Basic Gates

1. Aim

To design, construct and verify the truth table of a Full Subtractor circuit using basic logic gates / two Half Subtractors.

2. Theory

A Full Subtractor is a combinational circuit that subtracts two bits, A and B, taking into account a borrow input Bin from a previous subtraction stage, and produces two outputs: DIFFERENCE and borrow output Bout. The Boolean expressions are DIFF = A xor B xor Bin, and Bout = A'.B + Bin.(A xor B)', more commonly written as Bout = A'.B + A'.Bin + B.Bin, i.e., a borrow is generated if A is smaller than (B + Bin) in the corresponding binary subtraction.

A Full Subtractor can conveniently be constructed using two Half Subtractor circuits and one OR gate: the first Half Subtractor subtracts B from A to produce an intermediate DIFF1 and BORROW1; the second Half Subtractor subtracts Bin from DIFF1 to produce the final DIFF and an intermediate BORROW2; the final Bout is obtained by ORing BORROW1 and BORROW2. This modular construction mirrors the Full Adder and is used in binary subtractor circuits and arithmetic logic units.

3. Practical Set-up / Circuit Diagram

Fig. 13.1: Full Subtractor using two Half Subtractors and an OR gate

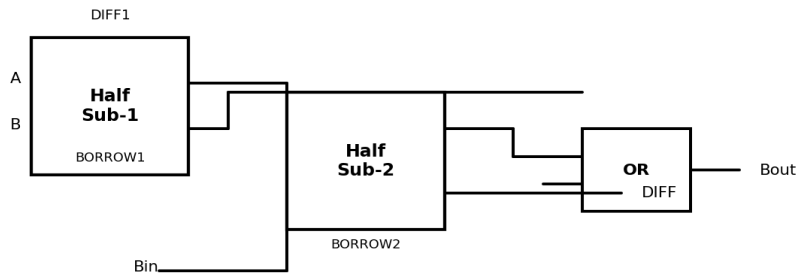

Fig. 13.1: Full Subtractor realised using two Half Subtractors and an OR gate

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7486 (XOR)	14-pin DIP	1
2	IC 7408 (AND)	14-pin DIP	1
3	IC 7404 (NOT)	14-pin DIP	1
4	IC 7432 (OR)	14-pin DIP	1
5	Digital IC Trainer Kit / Breadboard	with +5V supply, LEDs, switches	1
6	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Verify IC pin diagrams before wiring each gate stage.
- Ensure correct Vcc/GND connections to all ICs used.
- Cross-check the two Half Subtractor stages and OR gate wiring against the logic diagram before switching on.
- Do not leave any unused gate inputs floating.
- Switch off supply before modifying any connection.

6. Procedure

- Construct the first Half Subtractor with inputs A and B, producing DIFF1 and BORROW1.
- Construct the second Half Subtractor with inputs DIFF1 and Bin, producing the final DIFF and BORROW2.
- Connect BORROW1 and BORROW2 to the two inputs of an OR gate to obtain Bout.
- Apply all eight combinations of A, B and Bin (000 to 111) and note DIFF and Bout for each.
- Compare the observed truth table with the standard Full Subtractor truth table.

7. Observations and Calculations (Observations Table)

A	B	Bin	DIFF	Bout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

8. Results

The Full Subtractor circuit was constructed using two Half Subtractors and an OR gate, and its truth table was verified experimentally for all eight input combinations of A, B and Bin. The observed DIFF and Bout outputs matched the standard Full Subtractor truth table.

9. Viva Book

1. Write the Boolean expressions for DIFF and Bout of a Full Subtractor.
2. How is a Full Subtractor constructed from two Half Subtractors?
3. What is the significance of the borrow input Bin?
4. How is subtraction commonly implemented in ALUs using adders and 2's complement, instead of dedicated subtractor circuits?
5. Compare the structural similarity between a Full Adder and a Full Subtractor.

EXPERIMENT NO: 19

Test the Functionality of Multiplexer on Trainer Kit

1. Aim

To study the working of a 4:1 Multiplexer (MUX) and verify its truth table using a digital IC trainer kit.

2. Theory

A multiplexer (MUX) is a combinational circuit that selects one of several input data lines and routes it to a single output line, based on the binary value applied to a set of select lines. A 4:1 MUX (such as IC 74153, dual 4:1 line multiplexer) has four data inputs (I0-I3), two select lines (S1, S0) and one output Y, along with an active-low enable/strobe input. The relationship between the select inputs and the output is: Y = I0 when S1S0 = 00, Y = I1 when S1S0 = 01, Y = I2 when S1S0 = 10, and Y = I3 when S1S0 = 11, provided the enable input is active.

Multiplexers are widely used for data selection, data routing, parallel-to-serial conversion, and implementation of Boolean functions, since any n-variable Boolean function can be realised using a 2^n : 1 multiplexer with appropriate input line connections.

3. Practical Set-up / Circuit Diagram

Fig. 14.1: 4:1 Multiplexer — Trainer Kit Block Diagram

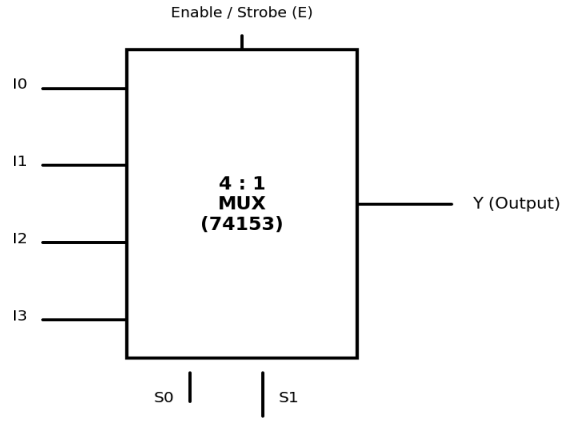

Fig. 14.1: 4:1 Multiplexer block/pin diagram (IC 74153) on trainer kit

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 74153 (Dual 4:1 MUX)	16-pin DIP	1
2	Digital IC Trainer Kit	with logic switches, LEDs, +5V supply	1
3	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Identify the IC 74153 pin diagram (data inputs, select lines, enable, output, Vcc, GND) correctly before wiring.
- Ensure the enable/strobe input is set to the active state required for normal operation.
- Do not leave unused data inputs floating; tie them to a defined logic level.
- Switch off supply before changing select-line or data-line connections.
- Verify connections against the pin diagram before applying power.

6. Procedure

- Connect the IC 74153 on the trainer kit with Vcc and GND connected correctly, and enable pin set active.
- Connect the four data inputs (I0-I3) to logic switches, and set them to fixed, distinct logic levels for testing.
- Connect the two select lines (S1, S0) to logic switches, and the output Y to an LED indicator.
- Vary the select line combination through 00, 01, 10, 11 and note which data input appears at the output each time.
- Verify that the output Y always matches the data input selected according to the select-line truth table.
- Repeat with different data input patterns to confirm consistent multiplexer operation.

7. Observations and Calculations (Observations Table)

S1	S0	I0	I1	I2	I3	Output Y (Observed)
0	0					
0	1					
1	0					
1	1					

8. Results

The 4:1 multiplexer IC was tested on the trainer kit, and its output was verified to correctly select the data input corresponding to each combination of the select lines, confirming proper multiplexer operation.

9. Viva Book

1. What is a multiplexer and what is its basic function?
2. How many select lines are required for an 8:1 multiplexer?
3. What is the purpose of the enable/strobe input in a MUX IC?
4. How can a multiplexer be used to implement a Boolean function?
5. Differentiate between a multiplexer and a demultiplexer.

EXPERIMENT NO: 20

Build and Test the Functionality of De-multiplexer on Trainer Kit

1. Aim

To study the working of a 1:4 De-multiplexer (DEMUX) and verify its truth table using a digital IC trainer kit.

2. Theory

A de-multiplexer (DEMUX) performs the reverse operation of a multiplexer: it takes a single data input and routes it to one of several output lines, based on the binary value applied to a set of select lines. A 1:4 DEMUX (such as one section of IC 74155, dual 2-to-4 line decoder/demultiplexer) has one data input (Din), two select lines (S1, S0), four outputs (Y0-Y3), and an enable input. When enabled, the data input Din is routed to the output line selected by S1S0 (e.g., Din appears at Y0 when S1S0 = 00, at Y1 when S1S0 = 01, and so on), while all other outputs remain at their inactive level.

De-multiplexers are widely used for data distribution, demultiplexing of communication channels, and (when the data input is tied to a fixed logic level) as line decoders for memory address decoding and other digital control applications.

3. Practical Set-up / Circuit Diagram

Fig. 15.1: 1:4 De-multiplexer — Trainer Kit Block Diagram

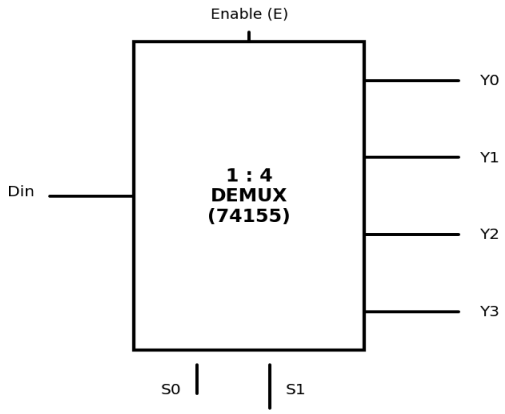

Fig. 15.1: 1:4 De-multiplexer block/pin diagram (IC 74155) on trainer kit

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 74155 (Dual 2-to-4 Decoder/DEMUX)	16-pin DIP	1
2	Digital IC Trainer Kit	with logic switches, LEDs, +5V supply	1
3	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Identify the IC 74155 pin diagram (data input, select lines, enable, outputs, Vcc, GND) correctly before wiring.
- Ensure the enable input is set to the active state required for normal operation.
- Connect LED indicators to all four outputs to observe the routing clearly.
- Switch off supply before changing select-line or data-input connections.
- Verify wiring against the pin diagram before applying power.

6. Procedure

- Connect the IC 74155 on the trainer kit with Vcc and GND connected correctly, and enable pin set active.
- Connect the data input Din to a logic switch and set it to a fixed logic level (e.g., logic 1).
- Connect the two select lines (S1, S0) to logic switches, and the four outputs (Y0-Y3) to LED indicators.
- Vary the select line combination through 00, 01, 10, 11 and note which output line reflects the data input each time.
- Verify that the data input consistently appears only at the output line selected by the select lines, with the remaining outputs inactive.
- Repeat with the data input set to logic 0 to further confirm correct demultiplexer action.

7. Observations and Calculations (Observations Table)

S1	S0	Din	Y0	Y1	Y2	Y3
0	0	1				
0	1	1				
1	0	1				
1	1	1				

8. Results

The 1:4 de-multiplexer IC was tested on the trainer kit, and the data input was verified to be correctly routed to the output line corresponding to each combination of the select lines, confirming proper de-multiplexer operation.

9. Viva Book

1. What is a de-multiplexer and how does it differ from a multiplexer?
2. How many outputs does a de-multiplexer with 3 select lines have?
3. How can a de-multiplexer be used as a line decoder?
4. What is the purpose of the enable input in a DEMUX IC?
5. Give a practical application of a de-multiplexer in digital communication systems.

EXPERIMENT NO: 21

Verify the Function of SR Flip-Flop using NAND/NOR Gate

1. Aim

To construct an SR (Set-Reset) flip-flop using NAND gates (and alternatively using NOR gates) and to verify its truth table, including the identification of the invalid/forbidden state.

2. Theory

An SR flip-flop is the most basic sequential logic memory element, having two inputs, Set (S) and Reset (R), and two complementary outputs, Q and Q'. It can be constructed using two cross-coupled NAND gates (active-low inputs, S' and R') or two cross-coupled NOR gates (active-high inputs, S and R). In the NAND-gate version, when S' = 0 and R' = 1, the flip-flop is Set (Q = 1); when S' = 1 and R' = 0, it is Reset (Q = 0); when both S' = R' = 1, the flip-flop holds its previous (last) state; and when both S' = R' = 0 simultaneously, an invalid/forbidden condition occurs since both Q and Q' try to become 1, violating their complementary relationship.

The NOR-gate version behaves in a complementary (active-high) manner: S = 1, R = 0 sets the flip-flop; S = 0, R = 1 resets it; S = R = 0 holds the previous state; and S = R = 1 is the invalid/forbidden state. The SR flip-flop forms the fundamental building block for more advanced flip-flops such as D, JK and T flip-flops.

3. Practical Set-up / Circuit Diagram

Fig. 16.1: SR Flip-Flop using cross-coupled NAND gates

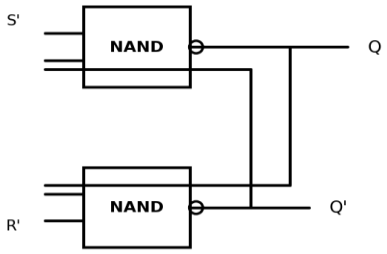

Fig. 16.1: SR Flip-Flop using cross-coupled NAND gates

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7400 (Quad 2-input NAND)	14-pin DIP	1
2	IC 7402 (Quad 2-input NOR)	14-pin DIP	1
3	Digital IC Trainer Kit / Breadboard	with +5V supply, LEDs, switches	1
4	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Cross-check the cross-coupled feedback connections carefully before switching on the supply.
- Avoid applying the invalid/forbidden input combination for an extended period.
- Verify IC pin diagram and Vcc/GND connections before wiring.
- Change only one input at a time while observing state transitions.
- Switch off supply before altering any connection.

6. Procedure

- Connect two NAND gates in cross-coupled configuration as shown in Fig. 16.1, with inputs S' and R' and outputs Q and Q'.
- Apply S' = 0, R' = 1 and note the state of Q and Q' (Set condition).
- Apply S' = 1, R' = 0 and note the state of Q and Q' (Reset condition).
- Apply S' = R' = 1 and verify that the flip-flop holds its previous state.
- Apply S' = R' = 0 briefly and observe the invalid/forbidden output condition; return immediately to the hold condition.
- Repeat the same procedure using two cross-coupled NOR gates with active-high S and R inputs, and compare the results.

7. Observations and Calculations (Observations Table)

S'	R'	Q	Q'	State/Remarks
0	1			Set
1	0			Reset
1	1			Hold (previous state)
0	0			Invalid/Forbidden

8. Results

The SR flip-flop was constructed using cross-coupled NAND gates (and verified alternatively with NOR gates), and its truth table was verified. The circuit was found to correctly Set, Reset and Hold its state as per the applied inputs, and the invalid/forbidden condition was identified when both inputs were simultaneously active.

9. Viva Book

1. What is the invalid/forbidden state of an SR flip-flop and why does it occur?
2. Compare the active levels of S and R inputs in the NAND-based versus NOR-based SR flip-flop.
3. What is meant by the 'hold' state of a flip-flop?
4. How is an SR flip-flop different from an SR latch versus a clocked SR flip-flop?
5. How can an SR flip-flop be converted into a D flip-flop?

EXPERIMENT NO: 22

Test the Functionality of D and T Flip-Flop using IC 7476

1. Aim

To configure and test a D (Data/Delay) flip-flop and a T (Toggle) flip-flop using the IC 7476 (dual JK flip-flop with preset and clear), and to verify their respective truth tables.

2. Theory

The IC 7476 is a dual JK flip-flop with additional preset (PR) and clear (CLR) inputs, triggered on the negative edge of the clock. Although it is inherently a JK flip-flop, it can be configured to behave as other flip-flop types by suitably connecting its J and K inputs. For a D flip-flop, the data input D is connected directly to J, and the complement of D (obtained through a NOT gate) is connected to K; on each active clock edge, the output Q then takes on the value of D at that instant (Q(next) = D), making it useful for data storage/synchronisation.

For a T (Toggle) flip-flop, the J and K inputs are tied together and driven by the single toggle input T. When T = 0, both J = K = 0 and the flip-flop holds its previous state; when T = 1, both J = K = 1 and the flip-flop toggles its output on every active clock edge (Q(next) = Q'). T flip-flops are widely used in binary counters and frequency division circuits, since each stage toggles at half the frequency of its clock input.

3. Practical Set-up / Circuit Diagram

Fig. 17.1: D and T Flip-Flop realised using IC 7476 (JK Flip-Flop)

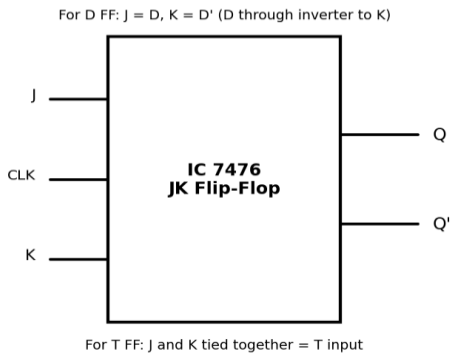

Fig. 17.1: D and T Flip-Flop realised using IC 7476 (JK Flip-Flop)

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	IC 7476 (Dual JK Flip-Flop)	16-pin DIP	1
2	IC 7404 (NOT gate, for D-FF)	14-pin DIP	1
3	Digital IC Trainer Kit	with clock source, LEDs, switches	1
4	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Identify the pin diagram of IC 7476 correctly, noting that it is negative-edge triggered.
- Ensure preset (PR) and clear (CLR) pins are held inactive (high) during normal clocked operation unless intentionally used.
- Apply clock pulses manually (push-button, debounced) or from a low-frequency clock source for clear observation.
- Verify J-K interconnections carefully for D-mode and T-mode configurations before switching on.
- Switch off supply before changing the flip-flop configuration.

6. Procedure

D Flip-Flop Mode

- Connect the data input D to the J input, and D through a NOT gate to the K input of the IC 7476, as shown in Fig. 17.1.
- Set D to a fixed value (0 or 1), apply a clock pulse, and note the resulting Q output.
- Repeat for the other value of D and confirm that Q follows D after each clock pulse.

T Flip-Flop Mode

- Tie the J and K inputs together and connect them to the toggle input T.
- Set T = 0, apply clock pulses, and verify that Q remains unchanged (hold state).
- Set T = 1, apply successive clock pulses, and verify that Q toggles (complements) with every clock pulse.

7. Observations and Calculations (Observations Table)

D Flip-Flop

Clock Pulse	D (input)	Q (before clock)	Q (after clock)
1	0		
2	1		

T Flip-Flop

Clock Pulse	T (input)	Q (before clock)	Q (after clock)
1	0		
2	1		
3	1		
4	1		

8. Results

The IC 7476 (JK Flip-Flop) was successfully configured and tested as both a D flip-flop and a T flip-flop. In D-mode, the output Q was observed to follow the data input D after each clock pulse. In T-mode, the output Q was observed to toggle with every active clock pulse when T = 1, and to hold its previous state when T = 0, confirming correct flip-flop operation in both configurations.

9. Viva Book

1. How is a JK flip-flop converted into a D flip-flop?
2. How is a JK flip-flop converted into a T flip-flop?
3. What is the function of the preset (PR) and clear (CLR) inputs in IC 7476?
4. What is meant by negative-edge triggering?
5. Why are T flip-flops commonly used in binary counter circuits?

EXPERIMENT NO: 23

Test the Functionality of DAC and ADC using IC

1. Aim

To study and test the functionality of a Digital-to-Analog Converter (DAC) using IC 0808 and an Analog-to-Digital Converter (ADC) using IC 0808/0809, by verifying their conversion accuracy for given digital/analog inputs.

2. Theory

A Digital-to-Analog Converter (DAC) converts a digital (binary) input code into a corresponding proportional analog output voltage or current. The IC DAC 0808 is an 8-bit multiplying DAC that accepts an 8-bit digital input (D0-D7) and produces an analog output current proportional to the binary input value, which can be converted to a voltage using an external op-amp based current-to-voltage converter. The output is given by Vout is proportional to (Digital input value / 256) x Vref, so that the digital code 00000000 corresponds to the minimum (zero) output and 11111111 corresponds to nearly the full-scale output.

An Analog-to-Digital Converter (ADC) performs the reverse operation, converting an analog input voltage into an equivalent digital (binary) output code. The IC ADC 0808/0809 is an 8-bit successive-approximation ADC with an 8-channel analog multiplexer, which samples the analog input, and through a successive-approximation register and internal comparator, generates the corresponding 8-bit digital output code after a start-of-conversion (SOC) pulse and an end-of-conversion (EOC) signal. Together, DACs and ADCs form the essential interface between the analog physical world and digital processing/control systems.

3. Practical Set-up / Circuit Diagram

Fig. 18.1: Block Diagram — DAC (0808) and ADC (0808/0809) Test Set-up

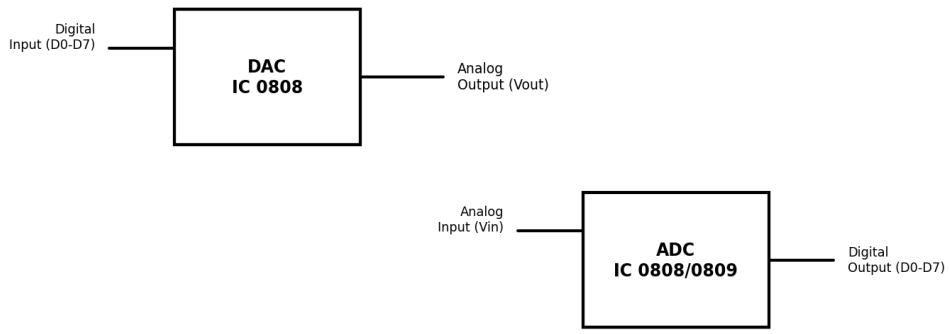

Fig. 18.1: Block diagram of DAC (IC 0808) and ADC (IC 0808/0809) test set-up

4. Apparatus Required

S.No.	Apparatus / Component	Specification / Range	Quantity
1	DAC IC 0808	8-bit Multiplying DAC	1
2	ADC IC 0808/0809	8-bit Successive Approximation ADC	1
3	Op-Amp (for I-to-V conversion)	IC 741	1
4	Digital IC Trainer Kit	with logic switches, LEDs, clock source	1
5	Digital Multimeter	0-20V DC	1
6	Connecting Wires	Single strand	As required

5. Precautions to be Followed

- Verify the pin diagram and reference voltage (Vref) connections of the DAC/ADC IC before wiring.
- Ensure the op-amp used for current-to-voltage conversion is biased correctly with dual supply, if required.
- Apply the Start-of-Conversion (SOC) pulse correctly and observe the End-of-Conversion (EOC) signal for the ADC.
- Do not exceed the analog input voltage range specified for the ADC IC.
- Switch off supply before changing digital input or analog input connections.

6. Procedure

DAC Testing

- Connect the DAC IC 0808 as shown in Fig. 18.1, with the 8-bit digital input connected to logic switches.
- Apply a known 8-bit digital code (e.g., 00000001) and measure the corresponding analog output voltage using a multimeter.
- Repeat for several digital input codes (e.g., 00000000, 01111111, 11111111) and tabulate the measured analog outputs.
- Compare the measured output with the theoretically expected value for each digital input code.

ADC Testing

- Connect the ADC IC 0808/0809 as shown in Fig. 18.1, with a known analog voltage applied to the analog input.
- Apply a Start-of-Conversion (SOC) pulse and clock signal, and wait for the End-of-Conversion (EOC) signal.
- Read the resulting 8-bit digital output on the LED indicators connected to the output pins.
- Repeat for a few different analog input voltages and tabulate the corresponding digital output codes.
- Compare the observed digital codes with the theoretically expected values for each analog input.

7. Observations and Calculations (Observations Table)

DAC

S.No.	Digital Input (8-bit)	Measured Analog Output (V)	Theoretical Output (V)
1	00000001		
2	01111111		
3	11111111		

ADC

S.No.	Analog Input (V)	Observed Digital Output (8-bit)	Theoretical Digital Output
1			
2			
3			

Calculations: DAC output Vout = (Digital Code / 256) x Vref; ADC digital code = round((Vin / Vref) x 256).

8. Results

The DAC IC 0808 was tested and found to produce an analog output voltage proportional to the applied digital input code, closely matching the theoretical values. The ADC IC 0808/0809 was tested and found to produce an 8-bit digital output code corresponding to the applied analog input voltage, confirming correct analog-to-digital conversion.

9. Viva Book

1. What is the resolution of an 8-bit DAC/ADC?
2. Explain the working principle of a successive-approximation ADC.
3. What is the significance of the reference voltage (Vref) in DAC/ADC circuits?
4. What are SOC and EOC signals in an ADC, and why are they needed?
5. Give two practical applications each of DAC and ADC in real-world embedded/control systems.